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MINIATURE ACTIVE MATRIX DISPLAY.(U)
JUL 78 J MURPHY, L J SIENKIEWICZ DAAK70-77-C-0140

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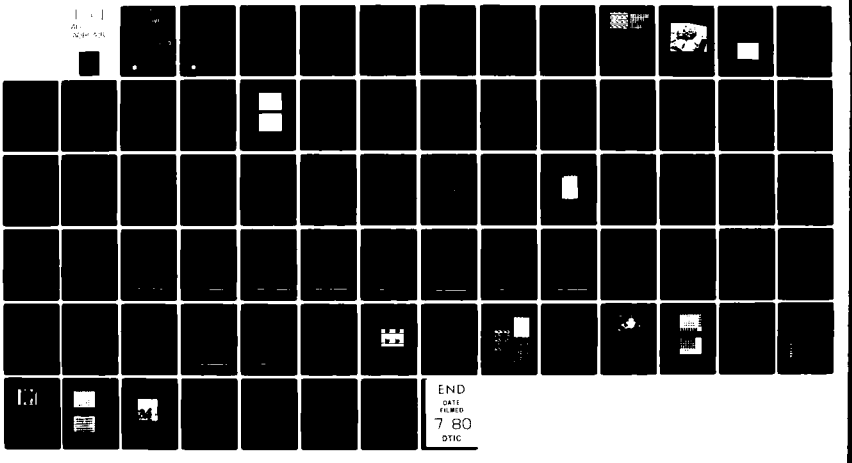

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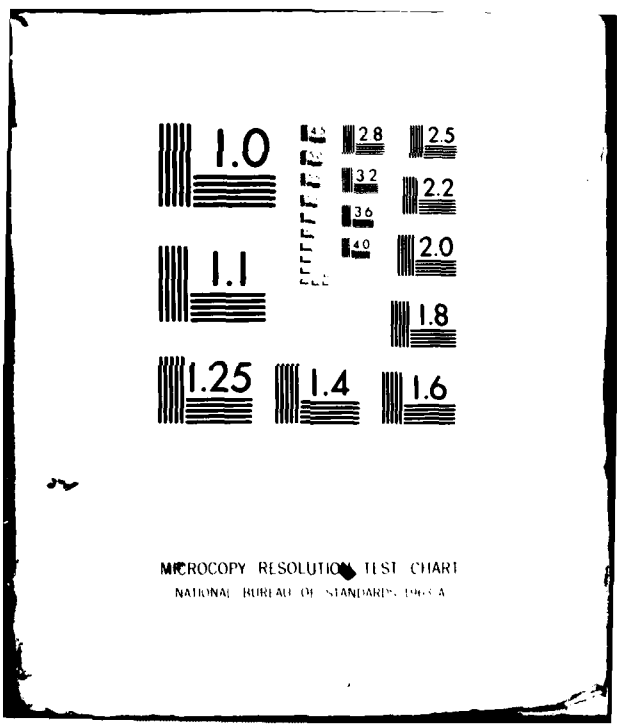
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MINIATURE ACTIVE MATRIX DISPLAY

Final Report on
Contract DAAK70-77-C-0140

LEVEL II

US Army Mobility Equipment
Research & Development Command
Ft. Belvoir, VA 22060

Contributors: J. Murphy and L. J. Sienkiewicz

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Pittsburgh, Pennsylvania 15235

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31 Dec 77 - 30 Jul '78

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1. INTRODUCTION

The purpose of this research is to take a step toward the development of a miniature flat panel display system in order to replace the miniature CRT now found in Helmet Mounted Displays. This research further attempts to advance projected uses in hand-held and weapon mounted target acquisition devices. The flat panel display would result in reductions in system size, volume, weight, power, voltage and cost relative to a CRT system. In addition, new system configurations would be possible as a result of the compactness of the flat panel system.

Flat displays using solid state electronics and various display media have already been developed as commercial products. In most of these, discrete light emitting or modulating elements are electronically addressed and activated. However, when high resolution is required, the large number of such elements results in difficult problems relating to element addressing, electrical connections, duty cycle, and power requirements. Over the past seven years, an intensive program at Westinghouse on the development of thin film transistor (TFT) circuits has made it possible to incorporate active circuitry within each display element, and has made it further possible to provide addressing with peripheral scanner circuitry in the same planar substrate as the display.

This new thin film technology has been successfully applied to displays using liquid crystals and electroluminescent display media, and its further application to a small, high resolution luminous display is a natural and promising extension of our past work.

The objective of this program was to develop fabrication methods for a high resolution active matrix. This program called for a laboratory model of an active matrix to be delivered at the end of the contract. The matrix would consist of no less than 100 x 100 pixels at

a linear pixel density of 400 ppi or greater coupled to some suitable display medium. It was intended that the successful completion of this program would be followed by a second phase in which the miniature display panel would be made with a linear pixel density, of 400 ppi or greater covering an area of about 1 square inch.

The present program is limited to the development of the techniques for fabricating high resolution active display panels. It includes a demonstration of the fabrication method but specifically excludes the development of associated drive electronics and display media.

Since memory thin film transistors (MTFT's) form the basis of the high resolution display panel, a discussion of the characteristics and drive considerations for MTFT's was considered to be a useful addition to the report and is included for the sake of completeness even though the work was done on earlier programs

The period of performance was originally from June 15, 1977 to December 31, 1977 with five months allotted to the experimental work and one month for report writing. Because of delays in various stages of the mask making process, several no-cost extensions were requested and granted and these extended the time to July 30, 1978.

2. TECHNICAL APPROACH

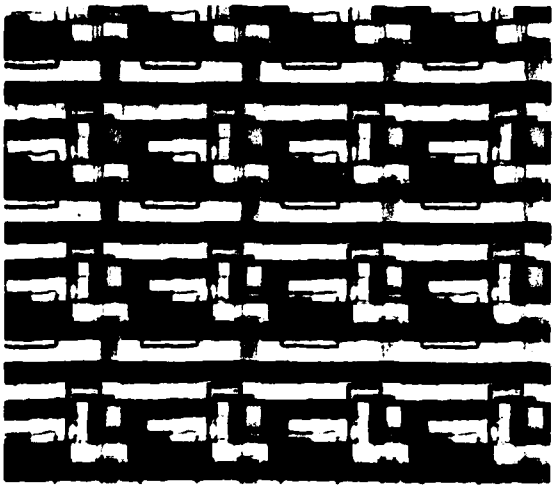
The fabrication methods employed in this program are an extension of the successful methods used previously by Westinghouse Research and Development Center in making low resolution (30-100 lines/inch) active display panels. These have been extensively documented in the literature and in contract reports.

2.1 OVERALL DESIGN CONCEPTS

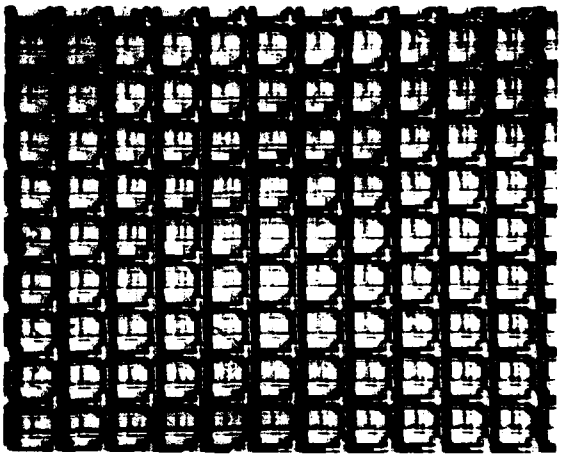
We used three key technical components in our efforts to construct a high resolution active matrix display, all proven at lower resolution:

- Thin film deposition techniques, employing two separate masking techniques
  1. micro-mask X-Y jig
  2. dedicated aperture masks.
- Thin film memory transistors, developed under Westinghouse and ONR funding, for maximum resolution.
- The proprietary Westinghouse hypermaintenance powder phosphors for long operational life, reliability and speed of response, with an option to employ thin film, high contrast phosphors at a later phase.

Each of the above components will be discussed in the following sections. With regard to high resolution masking techniques, Figure 2.1 shows a 256 x 128 array of TFT's (1 $in.^2$), developed under a NASA Goddard SFC contract. This array forms an optical computing plane, and the transistors at each picture point control the brightness of a phosphor dot--exactly as intended in this program.



(a) Portion of operational 256 x 128 TFT matrix, comprised of 128 x 128 cells over 1 in.^{2} Each cell contains two bus bars, two TFT's, and one PC element in 200 μm x 200 μm unit cell area.



(b) Portion of operational 100 x 100 TFT matrix over 1 in.^{2} Each cell contains two bus bars, one TFT, double layer capacitor, and output pad in 254 μm x 254 μm unit cell area.

Figure 2.1 — Examples of operational high resolution circuits.

The X-Y jig (Figure 2.2) is a miniature version of the one used in generating the large (6 x 6 in.) active matrices described in the literature, and consists of two independent X-Y movable planes, each plane carrying an identical, high precision mask containing a rectangular array of square apertures. By shifting one mask by a precisely controlled amount with respect to the other, identical rectangular apertures of different sizes and proportions as shown in Figure 2.3 can be generated. By shifting <u>both</u> masks with respect to the rigidly held deposition surface (e.g., glass), intricate rectangular film patterns can be generated, identical at every point; thus the required thin film network for the active matrix can be built up step by step.

This approach has been used to fabricate most of our active matrix circuits, including that shown in Figure 2.1. The jig shown in Figure 2.2 was used in the performance of the present work, with appropriately designed masks.

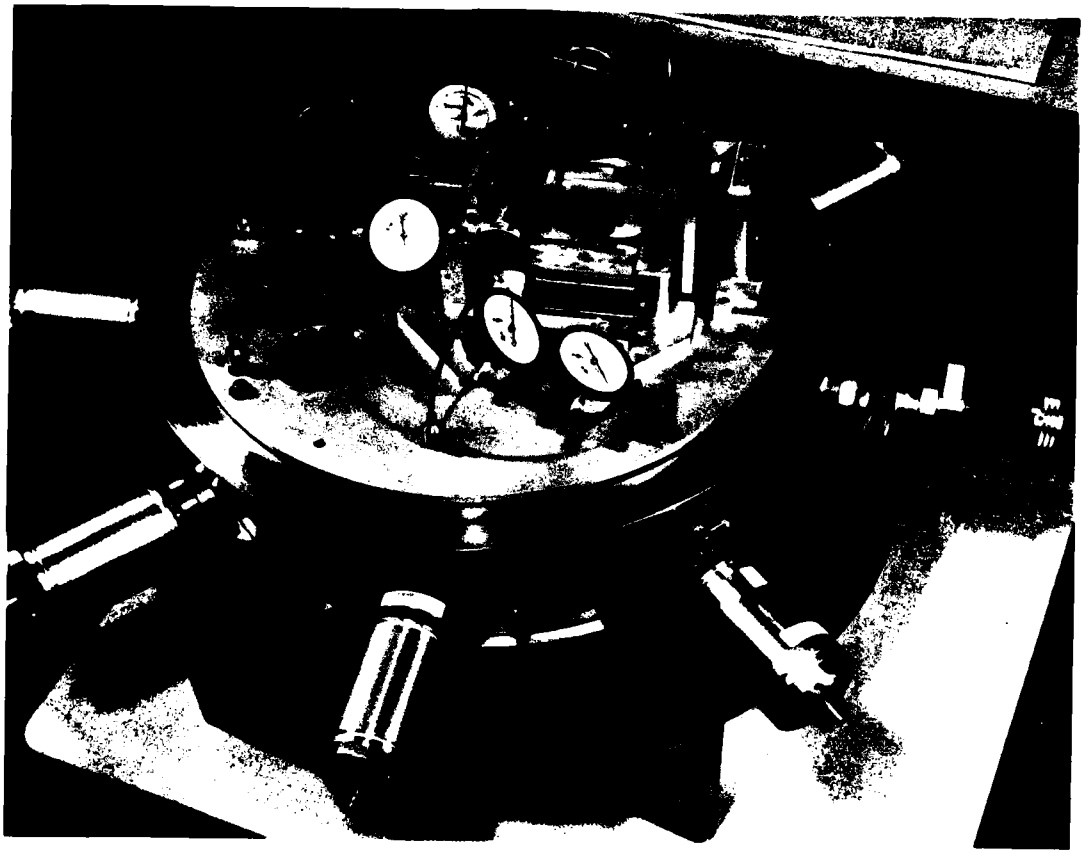


Figure 2.2. Westinghouse micro-mask jig.

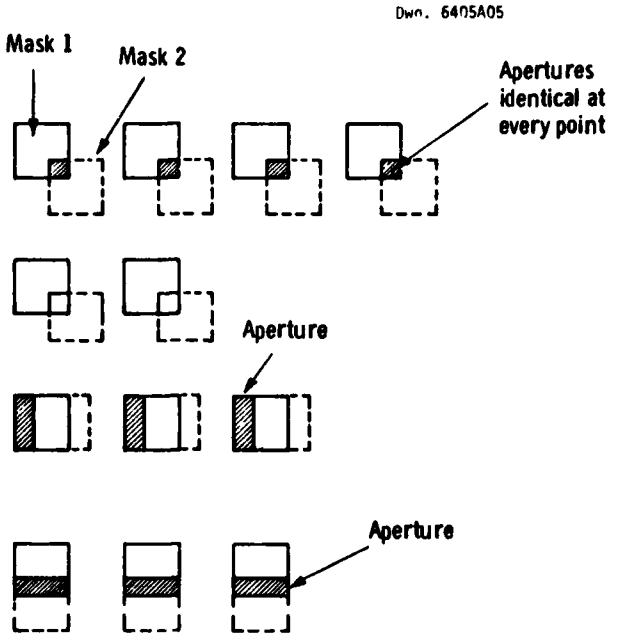


Figure 2.3--Principle of X-Y masking for display matrix synthesis

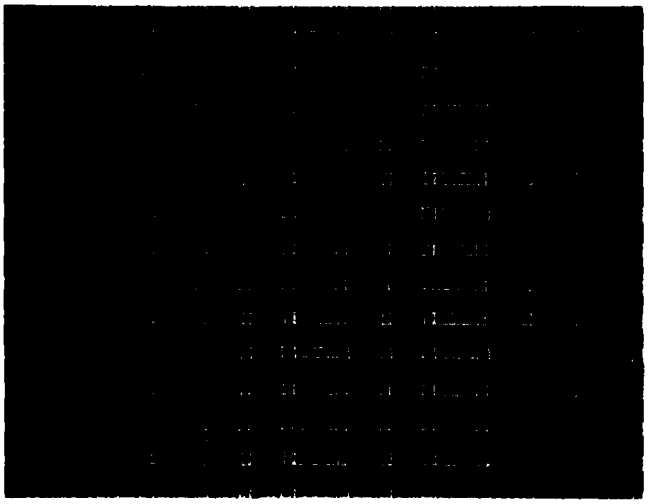


Figure 2.4. Photomicrograph of part of 1 in.^{2} 512 lines/inch with pattern of metal lines, generated in Westinghouse micro-mask jig.

Since an unusually short time was allotted to this project, we chose two parallel approaches and proceeded to work simultaneously on both of them. Parallel to the X-Y approach discussed above, the "dedicated mask" approach, in which the matrix circuit is embodied in a number of separate masks with different aperture configurations, was undertaken. This approach is closely related to the photomasking processes used in silicon circuit fabrication. The key technical problems with this approach occur as a result of the necessity of a good initial design, defect free masks, perfect mutual alignment of masks, and a high degree of perfection to the mask-to-substrate registration in the vacuum system.

Instead of the standard TFT's used in much of our previous display work, we proposed to utilize the memory TFT's, developed under ONR contract. Although a storage function was not specifically required in the proposed display, the use of the memory TFT's is highly advantageous because they permit the attainment of very high resolutions. This is because one can design an active matrix cell that contains only a single memory TFT (MTFT), instead of two normal TFT's, a storage capacitor, and an additional set of busbars needed for the active matrix driving an ac-excited phosphor. Indeed, without the MTFT, there would be no practical way in which an emissive display could be constructed at the needed 400 lpi or higher resolution. The design of the active matrix consisting of MTFT's will be discussed in Section 2.3; in Section 2.2, we provide an outline of the construction and physics of the MTFT device.

An added advantage of using MTFT's is the ease of testing the active matrix without the need for elaborate exercisers and multi-point edge contacts at very high resolution. Any other (non-memory) approach becomes much more difficult to test and evaluate at a stage prior to the development and full integration of the scanners and drive electronics.

The third key ingredient of our proposed display is the choice of a light-emitting rather than light-modulating display medium, and hence, the choice of a particular phosphor.

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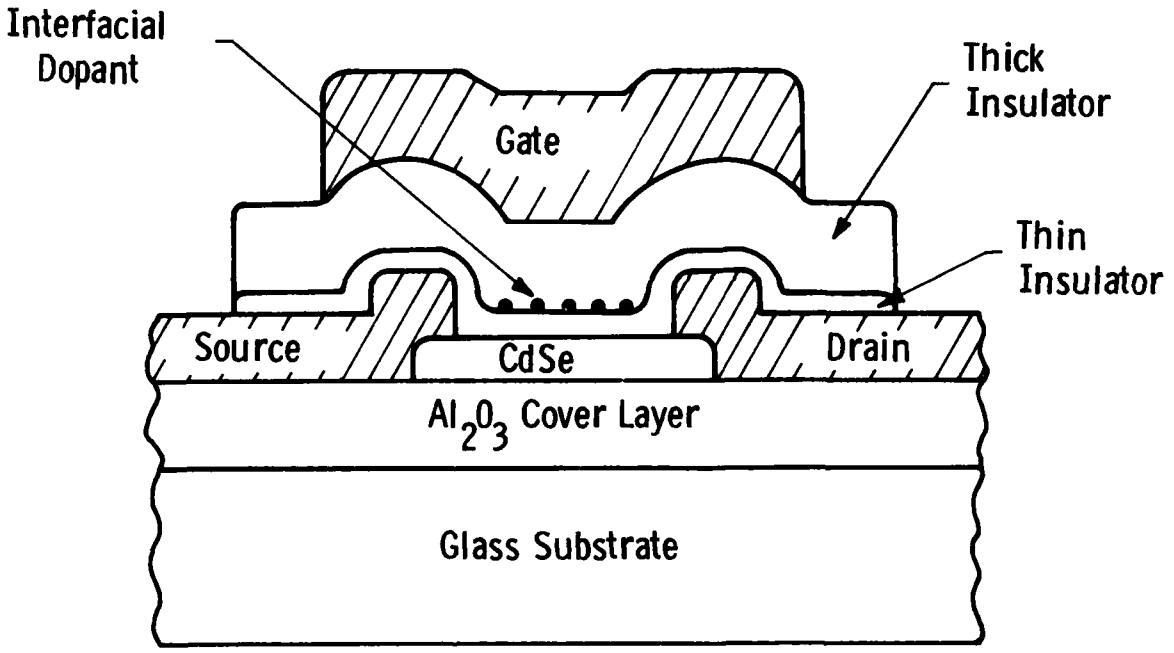

Interfacial
Dopant
Thick
Insulator
Gate
Thin
Insulator
Source
CdSe
Drain
Al_2O_3 Cover Layer
Glass Substrate

The reasons for choosing an EL-type display have, to an extent, already been alluded to. As mentioned in paragraph 1.3 of the RFQ, TFT matrices can indeed be designed to drive any display material, active or passive, while silicon matrices are necessarily restricted to passive LC-type materials, because of their inherent voltage limitations.

Later on, we will demonstrate the capabilities of the green Westinghouse hypermaintenance powder phosphors, and good lateral resolution, as well as the much better resolution of the high contrast thin film phosphor.

2.2 THIN FILM MEMORY TRANSISTOR

2.2.1 General Description

An active display matrix requires a component in each cell that stores the information regarding the brightness level (on-off or grey scale) for the display element in that cell. Space limitations at 400 lines/inch allow only one transistor and the light emitting element. Memory in the transistor was chosen since the development of memory in the light emitting medium was beyond the scope of the program.

The thin film memory transistor (MTFT) is an insulated gate field-effect transistor with an electrically alterable threshold voltage. Its principle of operation is similar to that of the Si MNOS memory devices in that the trapped charges in the gate insulator determine the transistor's threshold voltage. Figure 2.5 is a cross-sectional view of a basic MTFT structure. The CdSe is an n-type semiconductor of about 100 to 200 Å thick. The gate insulator structure is composed of a thick insulator (Al_2O_3) of about 1000 to 6000 Å, and a thin insulator (SiO) of about 100 Å. The interfacial dopant (IFD) is typically aluminum at a density of about 5×10^{15} atoms/cm^2 (equivalent to 10 Å). The metallization for the source, drain, and gate electrodes is typically 1000 Å of Au/In, but other suitable metals may be used. Although the drawing shown in Figure 2.5 indicates a gate structure only on the top side of the semiconductor, actual devices usually have another identical gate structure on the bottom side of the semiconductor. The additional bottom gate increases the performance of the transistor, and gives added stability protection to the CdSe surface.

2.2.2 Fabrication

Once the glass substrate is cleaned, all the fabrication processes are performed inside the vacuum system in one single pumpdown. The various parts of the device are deposited sequentially one layer after another onto the substrate through appropriate metal masks. A mask changer and mask-to-substrate registration system is installed inside the vacuum chamber and is controlled from the outside by electromechanical means. Cross-sectional views of a memory TFT through various stages of preparation are schematically illustrated in Figure 2.6 .

2.2.3 Device Characteristics

The CdSe TFT is an n-channel FET with ohmic contacts for the source and drain. Both enhancement and depletion mode devices can be fabricated by altering the CdSe film deposition condition and/or by appropriate doping of the semiconductor with indium. The memory TFT differs from the regular TFT only in the gate structure. Traps are created at the Al_2O_3-SiO interface by virtue of lattice mismatch. The presence of the aluminum IFD particles at this interface create extra traps that enhance the charging capability of the device. As a result, charging characteristics are much more controllable.

When a large enough WRITE voltage (V_W) of positive polarity is applied to the gate with respect to the source and drain, electrons are injected from the semiconductor into the traps, resulting in a net negative charge in the gate insulator even after the gate voltage is removed. As a result, the channel region of the semiconductor is depleted of an equivalent amount of electrons, causing the drain current to decrease. The corresponding threshold voltage (V_T) of the device then becomes more positive. Conversely, for a large enough negative V_W on the gate, the gate insulator is positively charged, resulting in an increase of drain current. The corresponding V_T is then shifted toward the negative direction. Figure 2.7 shows typical On/Off I-V characteristics (at zero gate bias) of a memory TFT at two

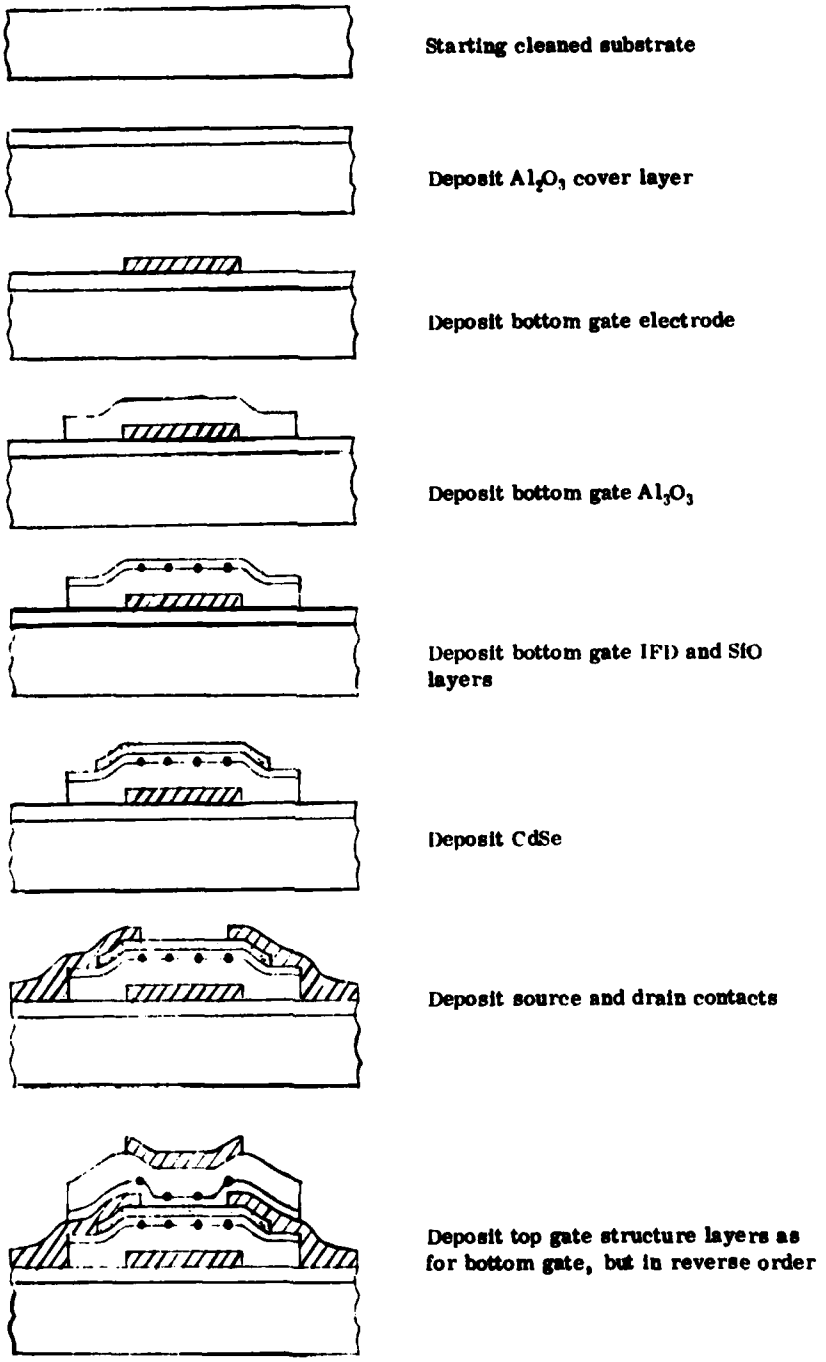


Figure 2.6. Deposition sequence of MTFT.

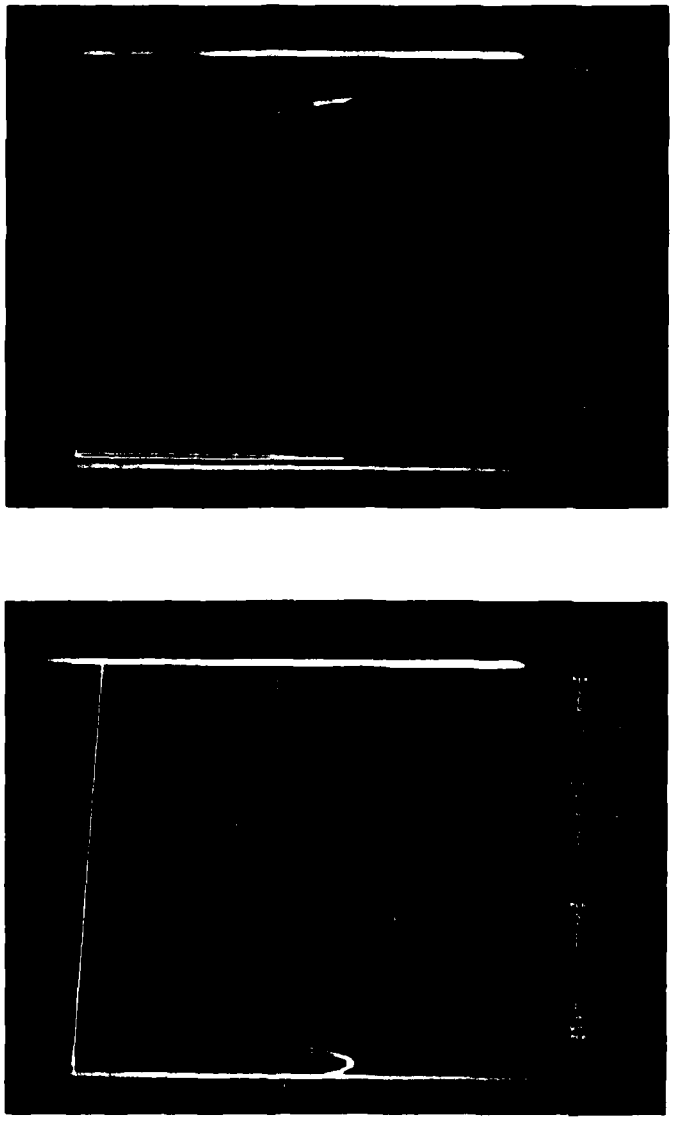


Figure 2.7. On/Off I-V characteristics of a memory TFT at two different scales. WRITE voltages: $\pm$ 30 V, 1 s.

different current scales. The "On" and "Off" states were obtained with WRITE voltages of minus and plus 30 V respectively.

However, the memory TFT is not limited to digital On/Off levels. Intermediate states can be obtained by appropriate adjustment of the WRITE voltage amplitude or the WRITE time. Figure 2.8a illustrates a typical dependence of V_T on V_W for a fixed WRITE time. This hysteresis behavior is referred to as the static WRITING characteristics of the memory TFT, as distinguished from the usual transient WRITING characteristics shown in Figure 2.9 , in which V_T is recorded as a function of WRITE time for a given V_W. This figure shows two WRITING curves for each polarity of V_W, each starting from a different initial V_T. The two positive V_W curves gradually merge together and saturate nicely. The saturation time of about 10 μs is comparable to the fast type MNOS devices. The negative V_W curves are much slower than the positive curves and show no tendency of saturation or merging even up to 10 ms. This slow negative WRITE phenomenon will be discussed further in the following paragraph. The charge retention capability of the memory TFT is illustrated in Figure 2.8b,in which the transistor's resistances in the "On" and "off" states are recorded as a function of retention time. The resistance was measured at low source-drain voltages with zero voltage on the gate. In between the resistance measurements, all terminals were grounded.

Aside from the transient negative WRITE behavior, all other characteristics of the CdSe memory TFT are similar to those of Si MNOS memory devices. Several possible explanations exist for the slow negative WRITE behavior shown in Figure 2.8a:

- One possibility is that the trapped electrons are deep and difficult to remove.
- The second plausible explanation is that holes are needed to neutralize the trapped electrons, and that the flow of holes is limited in the CdSe film.
- The third possible cause is the leakage of electrons from the gate metal to the traps that partially compensate for the

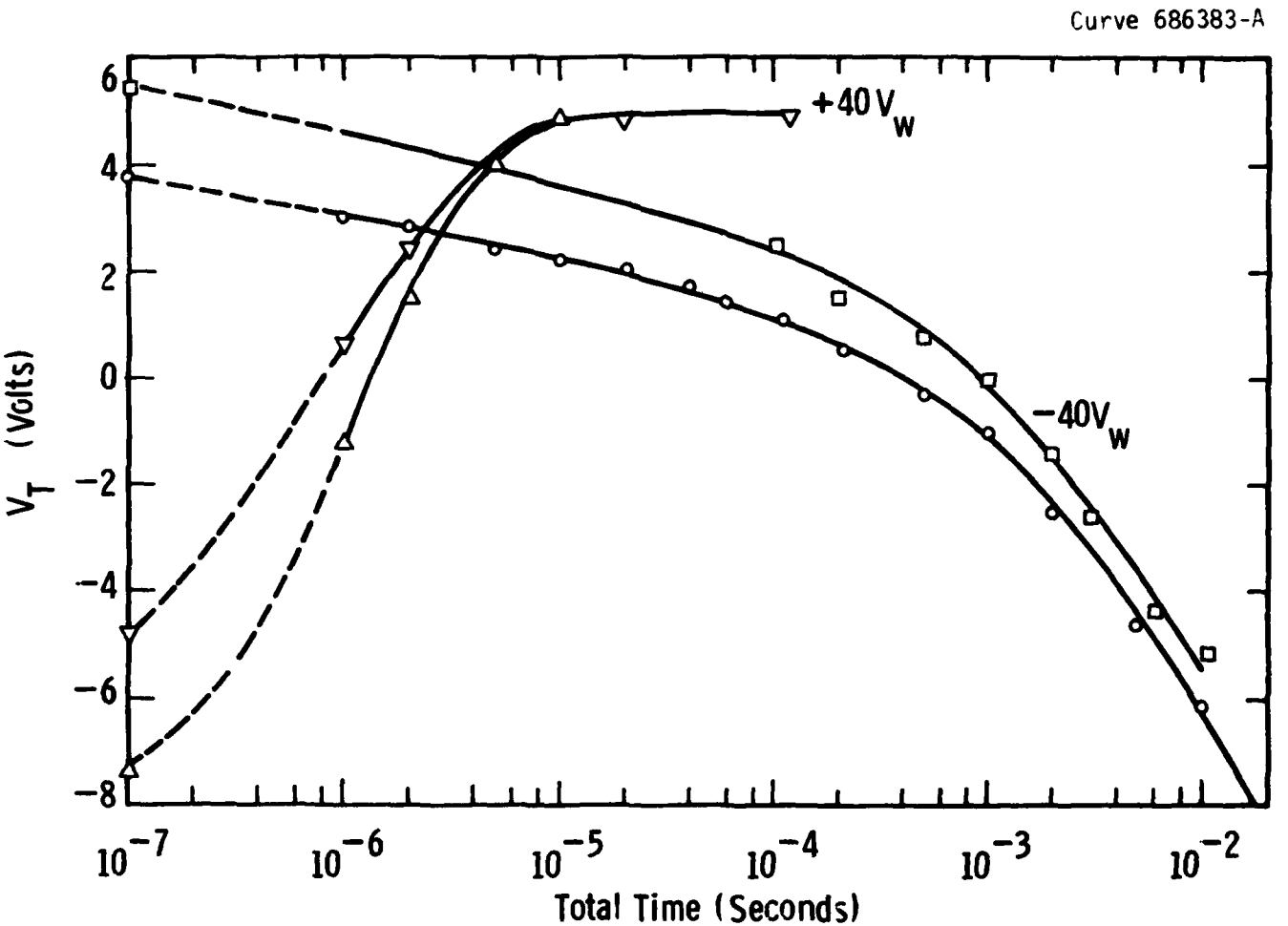


Figure 2.8a. Static WRITE characteristics of a memory TFT. Threshold Voltage versus WRITE. For each polarity, two curves are shown, each time starting from a different polarity.

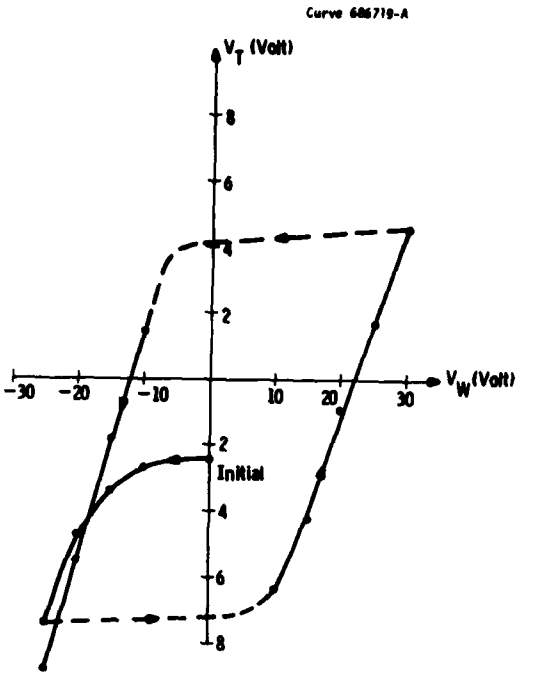


Figure 2.8b Static WRITE characteristics of a memory TFT. Threshold voltage versus WRITE voltage

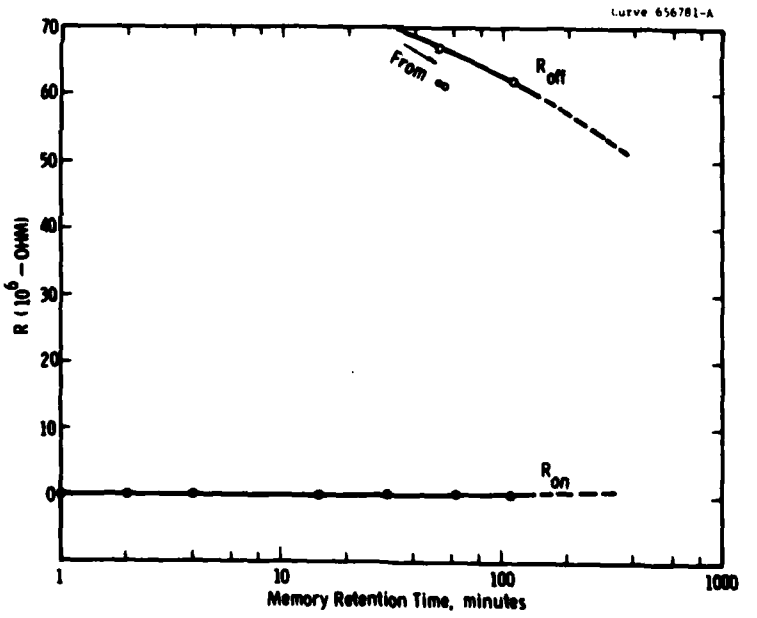


Figure 2.9. Transient WRITE Characteristics of a memory TFT. Threshold Voltage versus WRITE Time

electrons leaving the traps.

- The fourth possibility is the high channel impedance of the device during the negative WRITE cycle that effectively reduces the electric field across gate insulators.

We currently favor the high channel impedance model for the slow negative WRITE behavior. Further efforts will be necessary to confirm this hypothesis. As discussed in the following Section 2.3, the slow negative WRITE property does not prevent operation at video frame rates.

2.3 DESIGN AND ANALYSIS OF ACTIVE MATRIX USING MTFTs

Although this contract does not call for the development of drive circuitry, it is appropriate to describe the circuitry to be used with memory transistors so that the active matrix can be made more comprehensible.

Figure 2.10 depicts a 5 by 5 element portion of the active matrix. Each picture element in this matrix consists of an electroluminescent light emitting capacitor (C_{EL}) and a single thin film memory transistor (T_M). Each electroluminescent capacitor is connected between the drain electrode of the transistor and a common transparent front electrode of the display matrix. The source electrodes of all memory transistors in a row are connected to a row bus (Y_j) and the gate electrodes of all transistors in a column to a column bus (X_i). These buses serve as return paths for the electroluminescent excitation signal as well as for erasing and writing video information on the display matrix. As the individual device characteristics and the operating mode of the display matrix are determined by each other, the preliminary design specifications (Table 2.1) for both have to be considered.

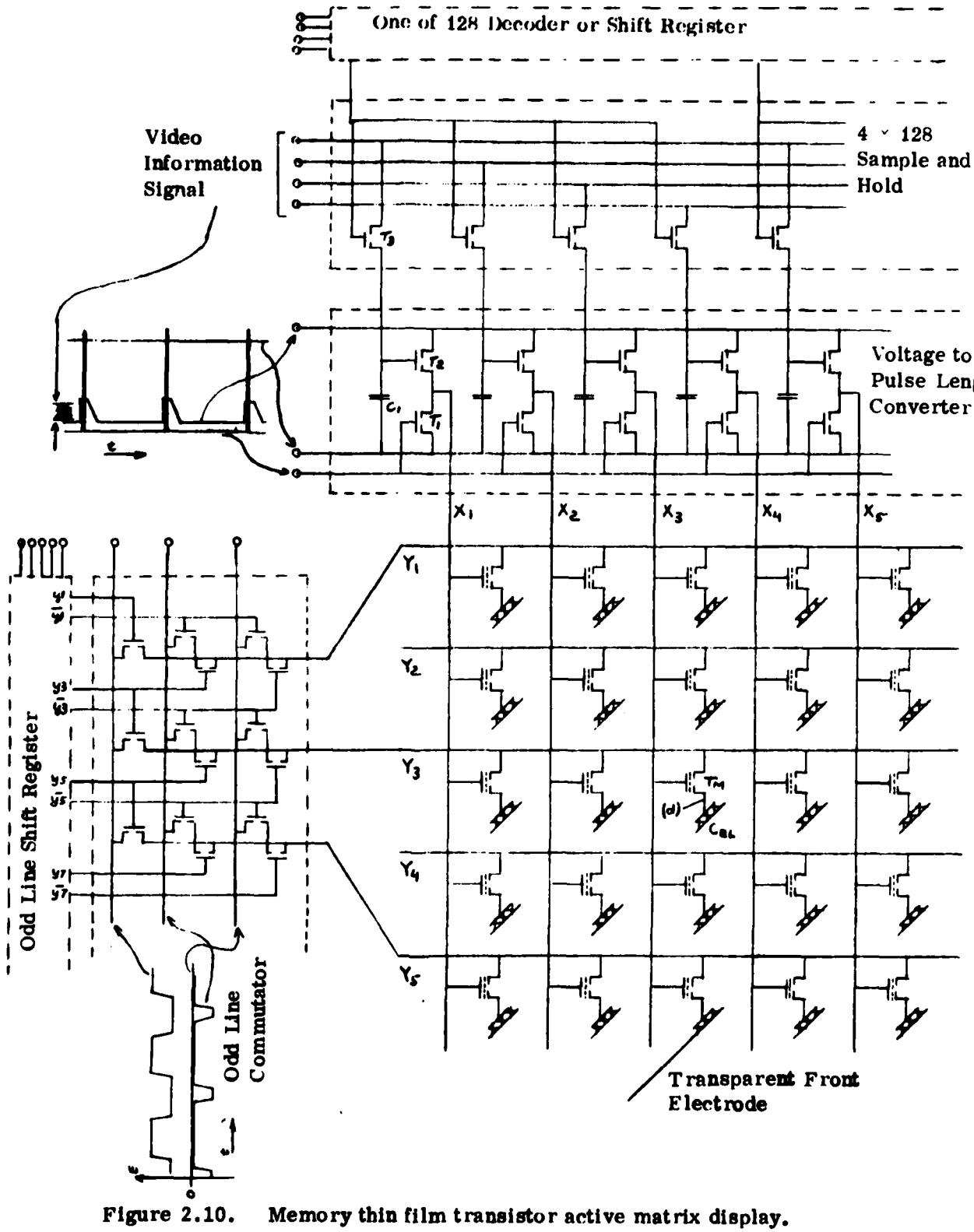


Figure 2.10. Memory thin film transistor active matrix display.

The following operating mode of the display matrix illustrated in Figures 2.11 and 2.12 is compatible with the above device characteristics and the real-time standard television video information format. In this operating mode, both previously stored information is erased and new information is stored on a matrix line-or row-at-a-time basis. As video information is received in real time for line j (j is even for even fields and odd for odd fields), it is sampled and stored as potentials in a 512-element sample and hold circuit as illustrated in Figure 2.10. At the same time, erase waveforms are applied to line j and m-1 succeeding lines in the same field, as illustrated in Figure 2.11 (if j+m-1 exceeds 512, lines at the beginning of the next field are erased). An approximate value of 128 for m, subject to optimization, is compatible with other specifications for the panel. A 75-V peak-to-peak replica of the 120-V peak-to-peak electroluminescent excitation waveform with a positive 100-V bias is applied to buses Y_j through Y_{j+2m-2} in the same field for erasing the corresponding lines. Figure 2.12B illustrates matrix point potentials at the beginning of an erase cycle (third line period) and Figure 2.12C at the end of an erase cycle (second line period). It can be noted that during 25 μs (approximately) of each horizontal line period, the transistor gate is negative with respect to source and drain electrodes by the required 140V. An accumulation of 128 such erase pulses will provide 3 ms, which is adequate for complete erasure of the transistor memory to the high conductance state. We also observe that a negligible amount of current, due to back bias, flows through the transistors during the erase cycle, and as a result, the corresponding electroluminescent elements will be dark. In addition to sampling video information and erasing previously stored information from m matrix rows, the stored information in the remaining matrix rows (384 for m = 128) is displayed as illustrated in Figure 2.12. The resulting 75% duty cycle and 14 fL peak brightness will provide the necessary 10 fL average brightness. Figure 2.12E illustrates a low conductance state stored in the memory transistor and therefore low light output from the corresponding electroluminescent cell or capacitor. It should be further noted that with zero current in the

Table 2.1 -- Preliminary Design Specifications

A. Electroluminescent Element Specifications

14 fL at 120 volt peak-to-peak 16 kHz excitation.

0.09 pF per element capacitance.

B. Memory Thin Film Transistor Specifications

0.05 μA saturated current in high conductance state with zero gate bias.

0.02 μA saturated current in low conductance state with zero gate bias.

140 volts positive gate pulse for 5 μs or less is required to change from high to low conductance state.

140 volt negative gate pulse for cumulative 3 ms or less is required to change from low to high conductance state.

0.03 pF or less gate to drain capacitance for each memory transistor.

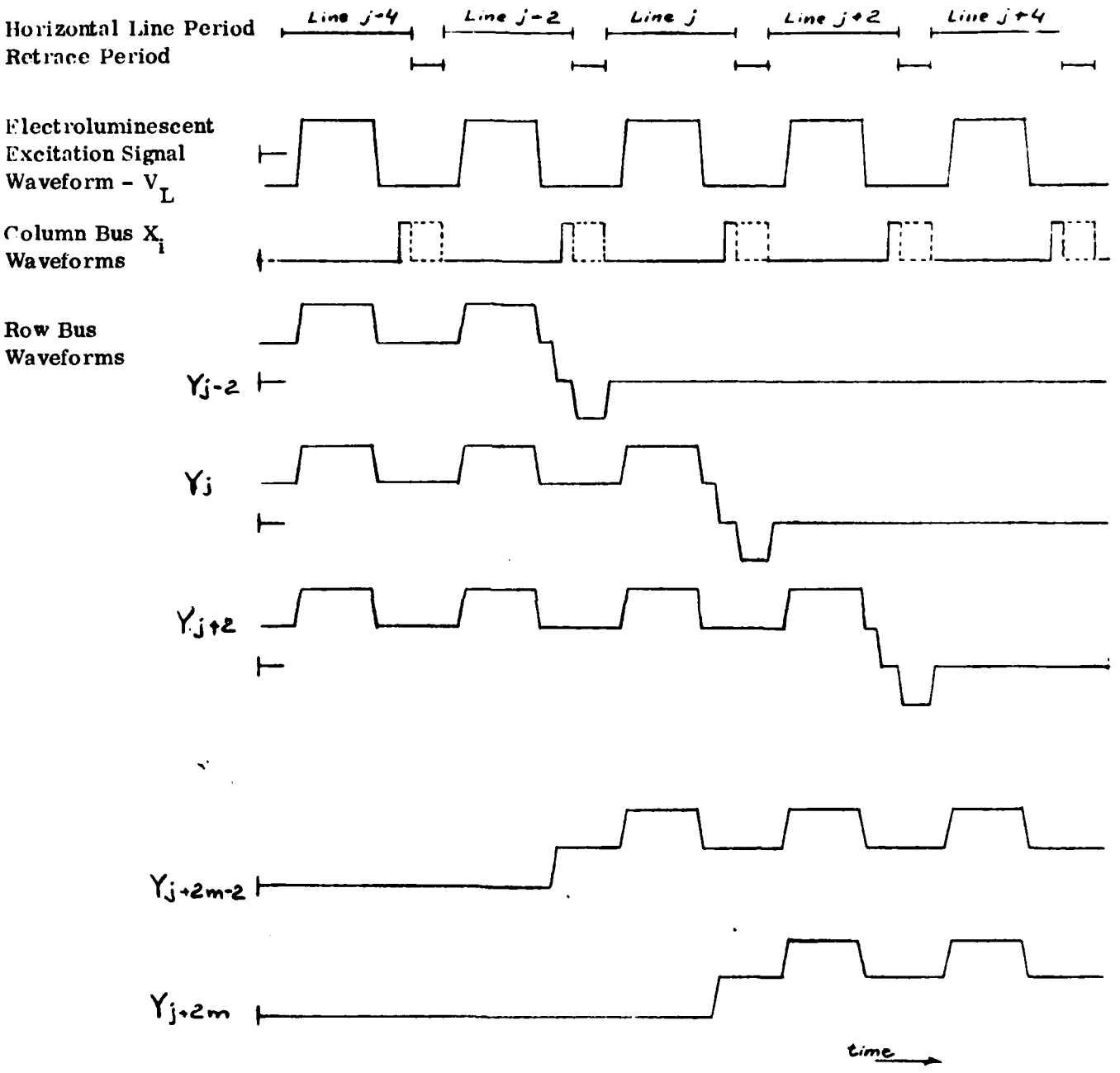


Figure 2.11. Memory thin film transistor matrix drive waveforms.

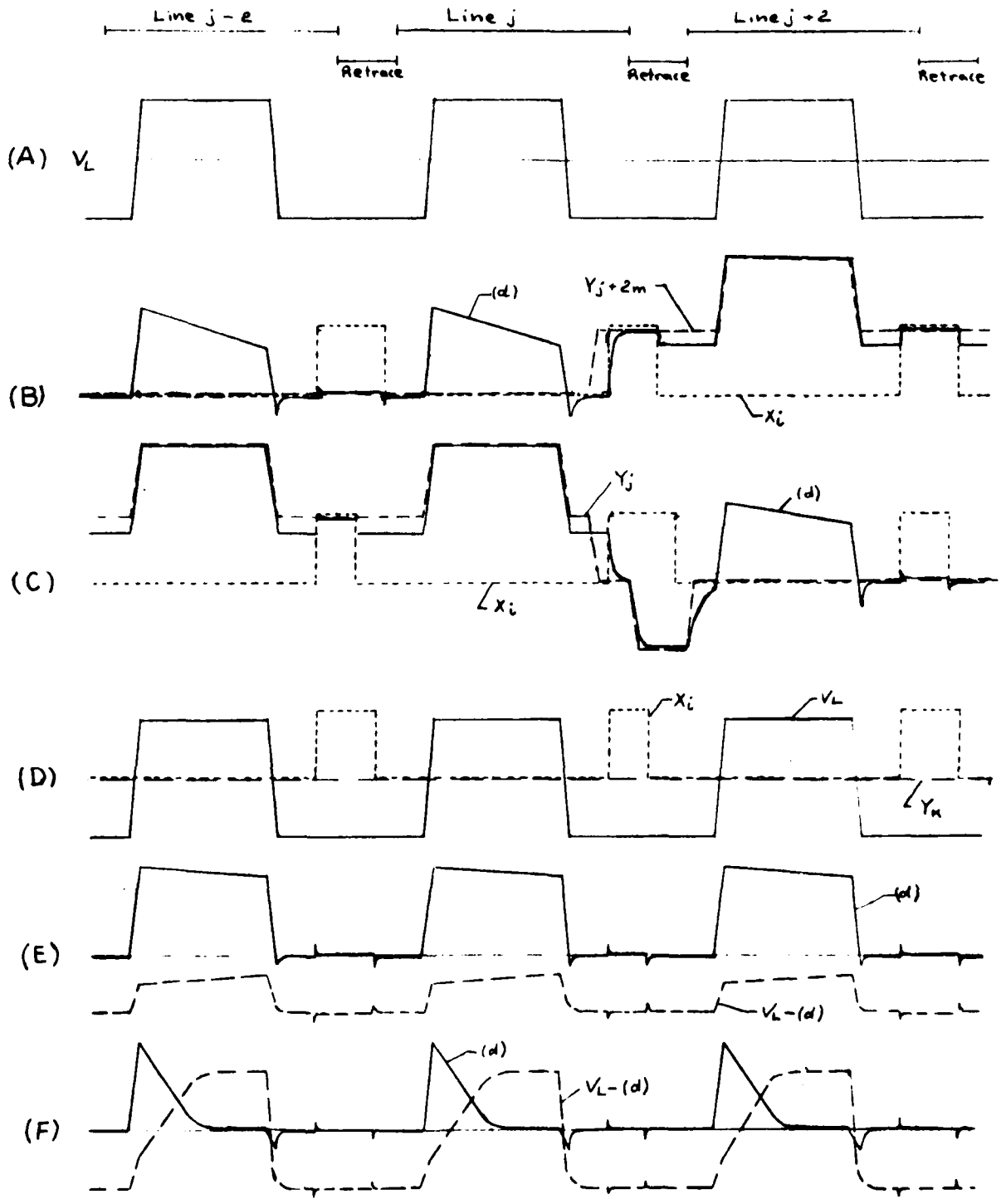


Figure 2.12. Memory thin film transistor matrix interior waveforms.

transistor, only a 30 V (approximately) peak-to-peak excitation signal will appear across the electroluminescent cell [(V_L-(d) where (d) is the instantaneous potential on the drain electrode of memory transistor, due to capacitive potential division between the electroluminescent capacitor and the gate-drain capacitance of the transistor. The threshold of the electroluminescent material prevents light emission at such low excitation. Figure 2.12F illustrates a high conductance state-store in the memory transistor. The drain electrode potential (d) decays to the source electrode potential (Y_K), which is held at zero, at least during a portion of the positive electroluminescent excitation cycle and the full 120-V peak-to-peak excitation (V_L) appears across the electroluminescent cell resulting in high light output. The intermediate conductance state stored in the memory transistors will produce intermediate light output levels.

At the end of horizontal line period for line j, a positive 70-V pulse is applied to all X_i buses as indicated in Figure 2.11 and Figure 2.12. These pulses serve two purposes. First, by imposing a positive gate potential on all memory transistors, they re-establish their drain electrode biases during the erase and display cycles. Second, the duration of these pulses and their time overlap with the negative 70 V row (Y_j) store pulses determine the conduction level stored in the memory transistors. The second retrace interval in Figure 2.12C illustrates the potential waveforms present at a matrix point during the period when information is transferred from the sample and hold circuit to the display matrix a line at a time. While the positive gate pulse (X_i) and the negative source pulse (Y_j) overlap in time, a positive 140 V gate-to-source and drain potential is imposed on the memory transistors. A short overlap as determined by gate pulse duration (X_i) will result in the retention of a high conductance state in the memory transistor. A maximum overlap of up to 5 μs will produce a minimum conduction state in the memory transistor.

While all of the above preliminary design parameters are based on experimental evidence, experimental data and geometric design specifications are insufficient for a calculation of the video voltage to light output transfer function at this time.

2.4 FABRICATION OF ACTIVE MATRIX

2.4.1 X-Y Jig Approach

Making an active matrix with the micro-mask jig shown in Figure 2.2, using the principles earlier described, is a straightforward though somewhat lengthy exercise. The main problem is the total number of deposition steps and actions that have to be taken by the operator, resulting sooner or later in a wrong setting or other human error, which effectively aborts the run. Nevertheless, with care and concentration,many perfect or very nearly perfect and functional matrices have been made in the past by this method, although at lower resolution.

Two somewhat different approaches were considered for the task. One was to use our existing 128 lpi mask set, but interpolate the settings in such a manner that the mask is shifted by only one quarter step at a time, and hence generate a pattern at 4 times the original density. The pattern of Figure 2.4 was generated in this way and shows the capability of the method. Although this method works, it has the disadvantage of requiring a large number of steps to complete the entire matrix, leading to a high probability of error somewhere along the line.

The other approach was to design a mask set more specifically for the present purpose. A mask design as illustrated in Figure 2.13 was completed prior to the start of this contract. The concept uses the top ("repertoire") mask for the definition of all the circuit patterns, while the bottom ("selector") mask is used as a shutter only, selecting one specific set of patterns for deposition at a given step.

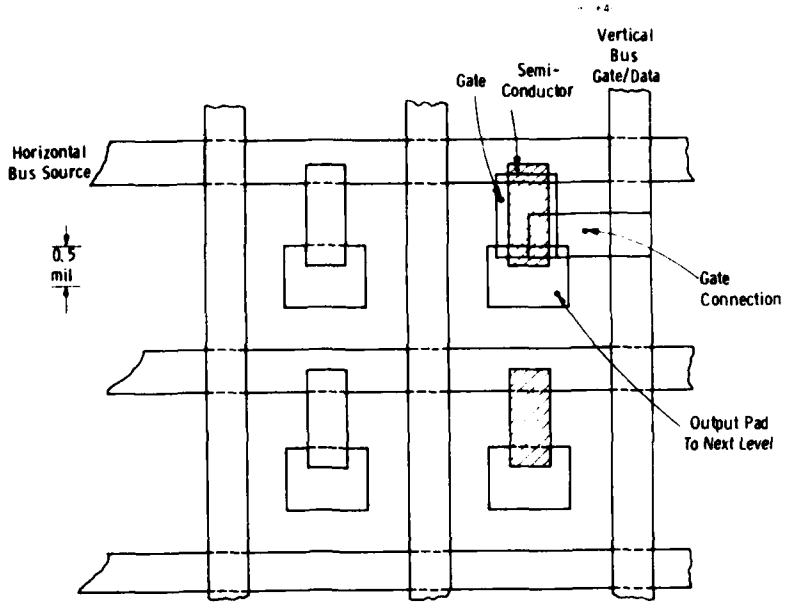


Figure 2.13. Circuit layout for 400 lpi memory TFT array

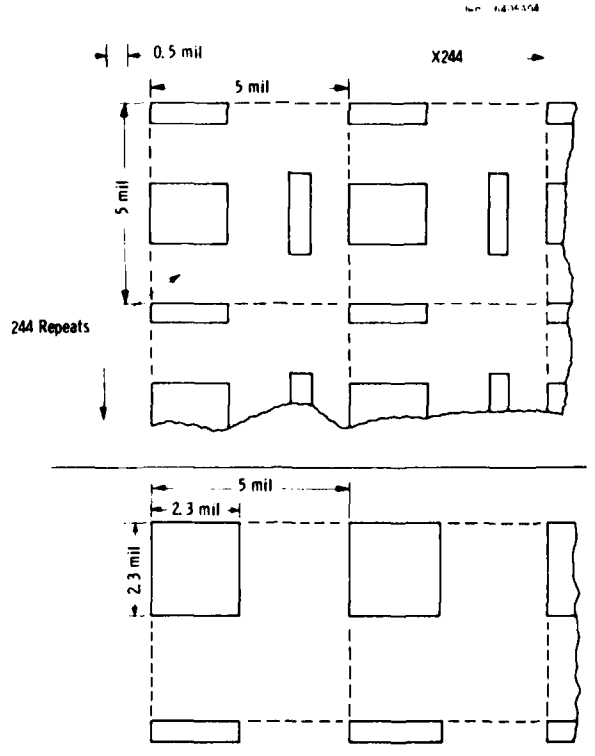


Figure 2.14. Layout of masks to fabricate matrix of Figure 2.13

Our mask suppliers (Towne Laboratories Inc.) confirmed that such masks could be made with their present technology. This mask set is designed for a somewhat lower (400 lpi) resolution, and requires a single interpolation only, i.e. the mask resolution is half the desired final resolution.

Figure 2.13 depicts a possible layout to realize the matrix circuit described in Section 2.3. This layout has the specific geometry which is realizable through the masks illustrated in Figure 2.14. The fabrication steps are listed in Table 2.2

After the active matrix is fabricated, a small number of additional steps will be needed to finish the display. These steps, which have been described in a published paper, will be summarized here. The steps are:

1. Photoresist application.
2. Exposure/development to generate 512 x 512 array of via holes.
3. Evaporation of output pads (for two-layer construction, to get large active display area).
4. Application of phosphor by spraying or brushing (or by evaporation of film-type phosphor).
5. Evaporation of semitransparent, common front electrode.
6. Front cover glass and seal.

Table 2.2--Fabrication Steps for Matrix Circuit of Figure 2.

Operation	Step
1, 2, 3	Vertical bus
4,5	Bottom gate
6,7	Gate, crossover insulators
8	Floating gate
9	Thin gate insulator
10	CdSe
11, 12, 13	Horizontal bus
14	Drain pad
15	Top gate insulator (thin)
16	Top floating gate
17, 18	Top gate

3. CIRCUIT DESIGNS

3.1 X-Y LAYOUTS

Two different circuit layouts for fabricating 256 cells per inch displays with 128 aperture per inch masks were designed. As discussed earlier, it is considered essential to develop the techniques for the higher resolution ($\gtrsim$ 400 cells/inch) at a lower resolution in order to determine the limitations of the method. The first layout is shown in Fig. 3.1.

The four-fold arrays were made by evaporating each pattern four times having shifted the X-Y masks to the appropriate locations. Some of the patterns shown in Fig. 3.1 are formed from multiple steps as is indicated by the overlapping or isolated areas. For example, in Fig. 3.1(a), the source-drain apertures require a setting for each source, an evaporation, a resetting of the masks to form the drain pad and the concomitant evaporation. The gates in Fig. 3.1(e) require double steps as well.

The procedure to form a 128 x 128 sub-array is as follows:

(1) Deposit the source-drains through aperture a1* (of Fig. 3.1).
(2) Deposit the semiconducutor through aperture b1.
(3) Deposit a thin layer of insulator (SiO) through c1.
(4) Deposit a thin layer of aluminum metal (10 $\sim$ 20Å) through the same aperture c1.
(5) Deposit a thick layer (6000Å) of Al_2O_3 through d1.
(6) Deposit the gate electrode through apertures e1.

*Label the elements of the four sub-arrays 1, 2, 3 and 4 reading counter clockwise from the top-right corner.

Dwg. 7688A07

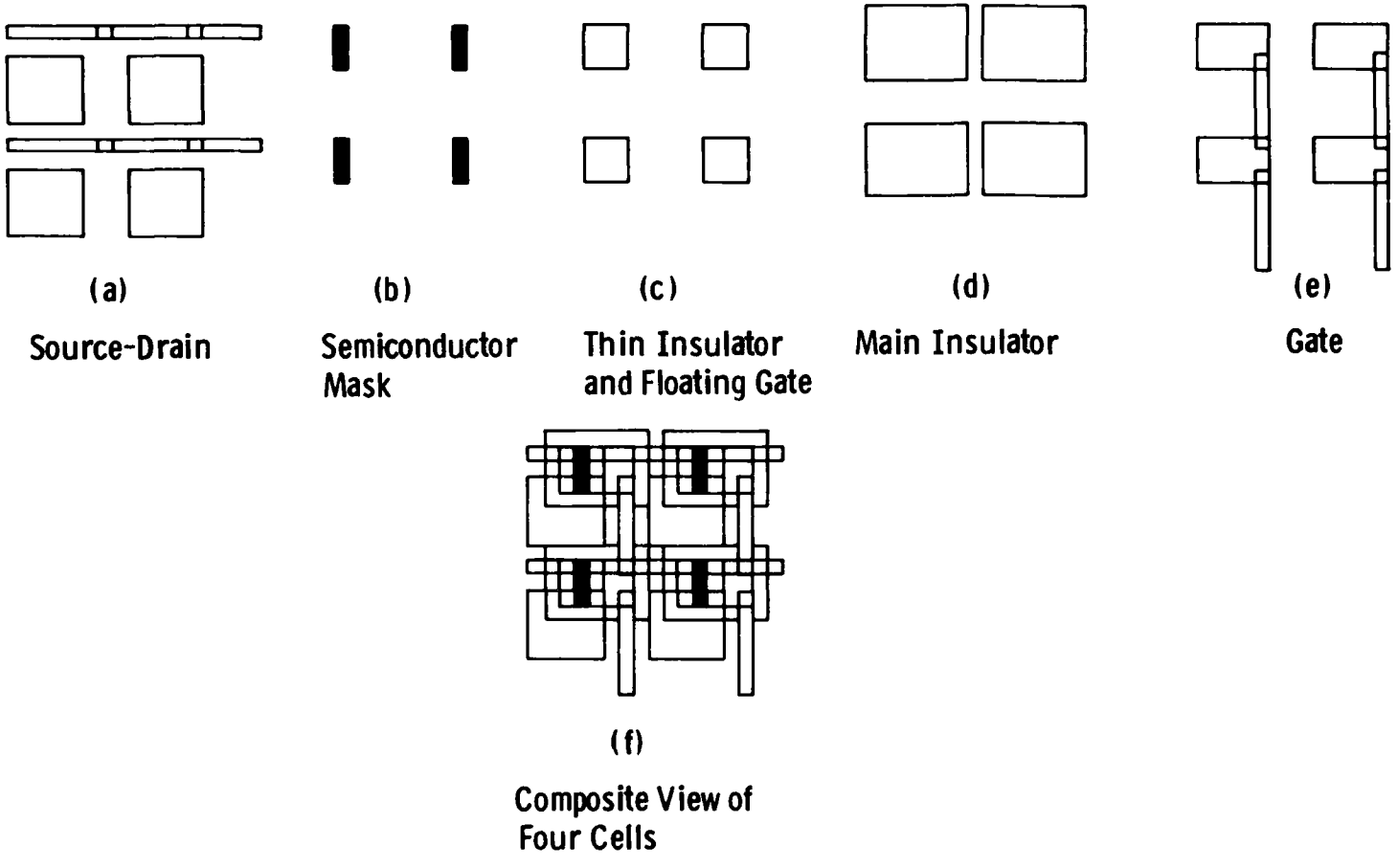
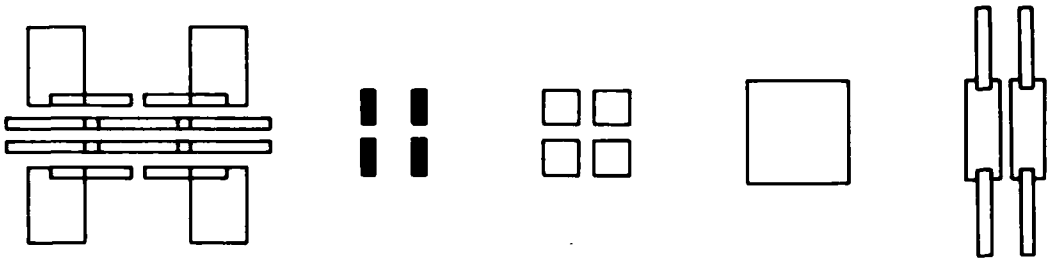


Figure 3.1
Aperture layouts for 256x256 per in^2 array using 128 x 128 per in^2 mask

Dwg. 7688A08



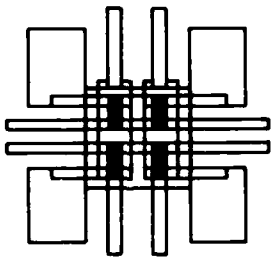
(a) Source-Drain

(b) Semiconductor

(c) Light Insulator and Floating Gate

(d) Main Insulator

(e) Gates



(f) Composite View of Four Cells

Figure 3.2
Alternate layout to Figure 3.1. This layout requires fewer deposition steps but has tighter tolerance limits on the mask movements

Because each sub array requires a completely separate set of evaporations, the complete array will require 56 sets of aperture adjustments. The array design is limited by the maximum available aperture which is 7/16 of the aperture spacing or .0034 inches. Since the complete transistor must fit into this space, the narrowest usable aperture is .0034/7 = .00049 inches for a total tolerance of $\pm$ .00024 inches between adjacent aperture edges.

The second layout (Fig. 3.2) uses four sub arrays with differing cell orientations so that four transistors are located in adjacent corners of the cells. This design has the advantage that the source bus, insulator, and interfacial dopant evaporation (i.e., the light aluminum layer after the SiO layer) can be shared among the sub arrays. The advantage of this arrangement over the former is that it requires only 32 sets of aperture adjustments. Furthermore, the groups of four drain output pads provide a larger target for opening the photoresist for second layer output pad contacts. The major disadvantage is that the tolerance on the aperture edges is reduced to $\pm$ .00019 inches because we must now squeeze four transistors within the area of a single insulator.

3.2 DEDICATED MASK DESIGN

The layout of the circuit is slightly different for the dedicated mask approach. In it, the gates become the row busses while the transistor sources are the column busses. After the basic layout was conceived it was developed on an Applicon graphics computer. The detailed aperture dimensions and artwork compensation were arrived at with the help of Towne Laboratories in Somerville, NJ, who subsequently made the metal masks. Eighteen photomasters were needed to make the nine metal masks required. The photomasters were made from Applicon computer tapes on the Mann 1600 high resolution pattern generator at the Westinghouse Advanced Technology Laboratories in Baltimore, MD. The average Mann generator run time was 20 hours per photomaster at approximately 7150 flashes per hour. The photomasters were then shipped to Towne Laboratories where the metal electroform nickel masks were made.

Figure 3.3 is an outline view of the masks showing where the target alignment, squares, check pattern, and area of detail for all of the masks (in later figures) is located.

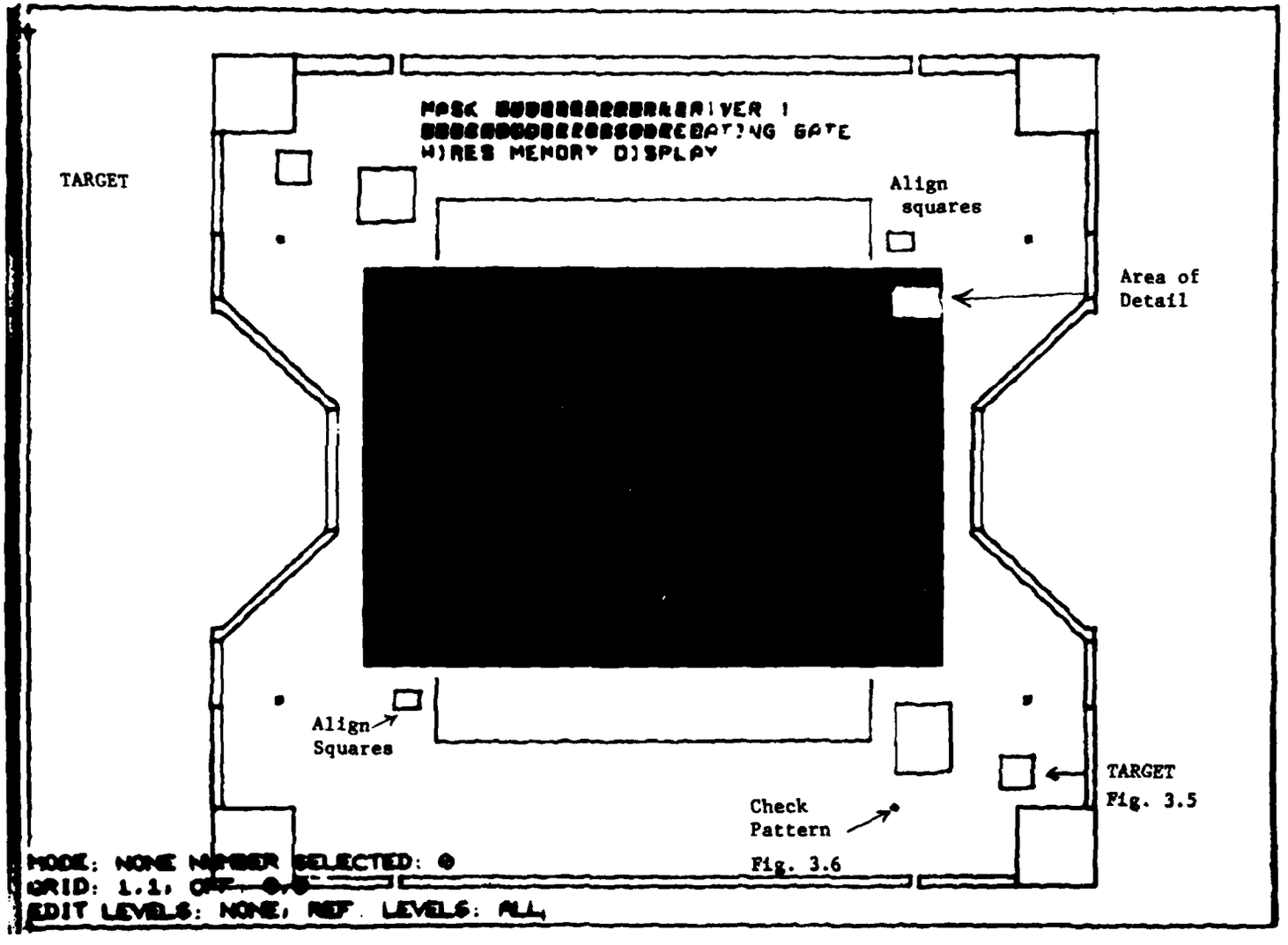


Figure 3.3 HIRES Memory Display - Outline View

Figure 3.4 shows the location of alignment squares on each mask. Mask #3 (Figure 3.10) is the reference mask with all large squares (50 μ) unless otherwise indicated. All other masks have small squares (30 μ) as indicated. For alignment a reference deposition is made of Mask #3 on a reference substrate. All other masks are aligned to the align squares on the reference substrate. The small square on Mask #1 is set inside of the corresponding large square on the reference substrate. This alignment procedure continues on all masks.

Figure 3.5 gives the target detail. It is used for aligning the defining and the relief side photomasters when making the tooling. The metal masks are made so that only one side is meant to be in contact with the substrate. This is called the defining side. The other side of the mask has a larger aperture than the defining aperture and it is called the relief side. The design of the target allows for alignment regardless of the polarity of the photo masks.

Figure 3.6 is the check pattern. When making the photomasters the Mann generator will flash a square at the target location prior to beginning the sequence of flashes for the photo mask. When the mask is completed, the generator returns to the target area and flashes the four outside squares of the target. The alignment of the completed target enables the user to determine whether or not run-out errors have occurred in the photo mask. The precision to which the target is aligned is a measure of the cumlative errors that have occurred during the making of the photo mask.

Figure 3.7 is a composite overlay of the masks showing how the deposited substrate would look. Duplicate masks are not shown in this view.

The complete set of masks for making the transistor array are listed in Table 3.1 and are shown in detail in Figures 3.8 to 3.14. The defining sides are shown cross hatched and the relief sides are shown clear. It will be noticed that the relief sides are shown with figures that do not appear to make the defining apertures in some cases. This occurs because the masks are made by a process that involves etching and plating up. In the process, apertures change size and shape. In order to compensate for these changes, the initial hole sizes are suitably adjusted. The compensations are determined empirically. The location of each mask relative to the completed pattern is shown in the accompanying "a" figures.

TABLE 3.1

HIRES MEMORY DISPLAY

Metal Mask No.	Function	Photomasters Required	Number Metal Masks Required Per Set
TL-100188-1	Vert IC #1 & source	Mark 1 & 1A	1
TL-100188-2	Vert IC #2 & source	Mask 2 & 2A	1
TL-100188-3	Horiz IC #1 & Gate	Mask 3 & 3A	1
TL-100188-4	Horiz IC #2 & Gate	Mask 4 & 4A	1
TL-100188-5-6	Insulator #1 & #2	Mask 5-6 & 5A-6A	2
TL-100188-7-8	Semiconductor	Mask 7-8 9-10 & 7A-8A 9A-10A	2
TL-100188-9-10	Floating Gate	Mask 7-8 9-10 & 7A-8A 9A-10A	2
TL-100188-11-12	Drain	Mask 11-12 & 11A-12A	2
TL-100188-13	EL contact	Mask 13 & 13A	1

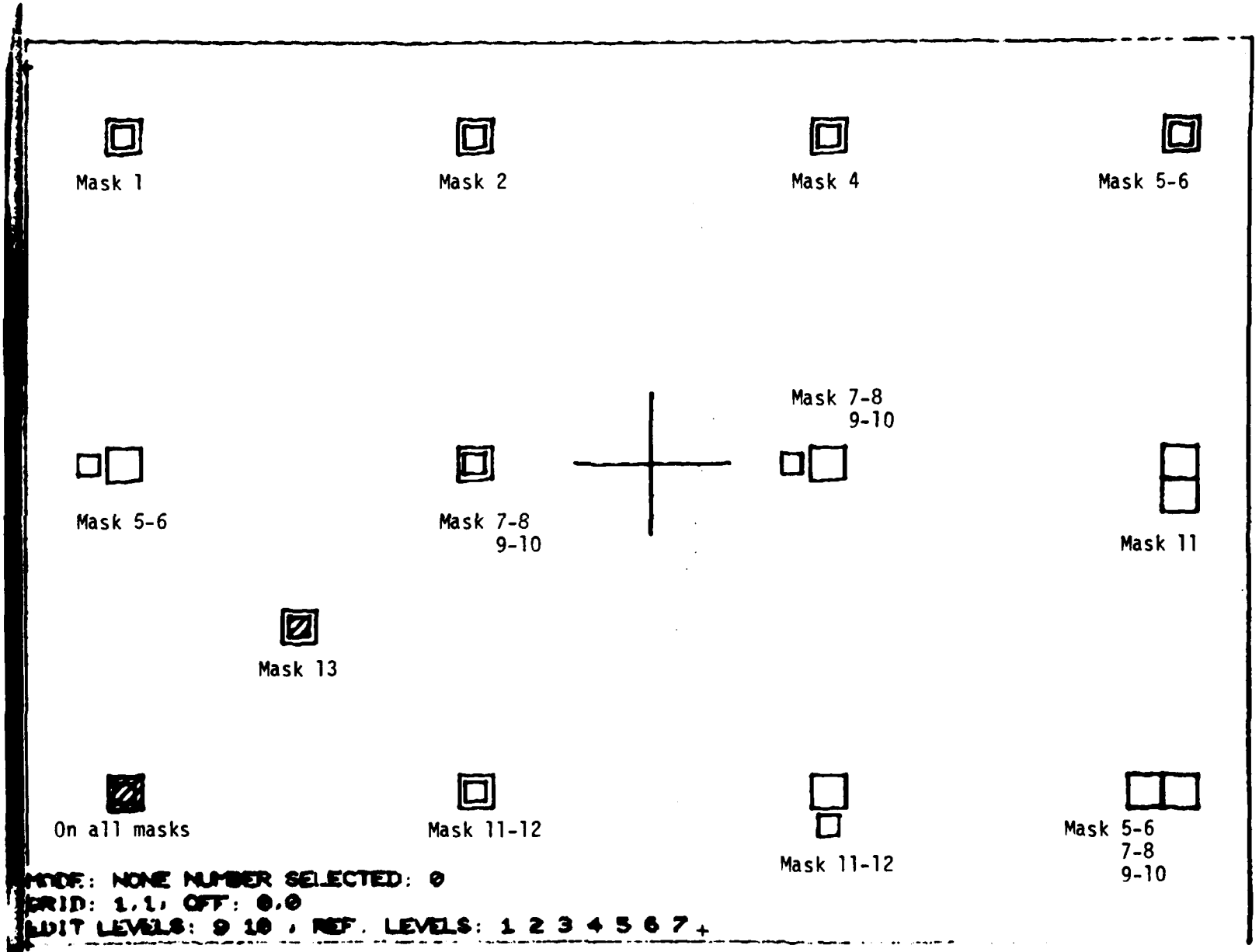


Figure 3.4 HIRES Memory Display

Large square = 50 μ
Small square - 30 μ
Large squares on Mask 3
unless indicated otherwise
Small squares as indicated

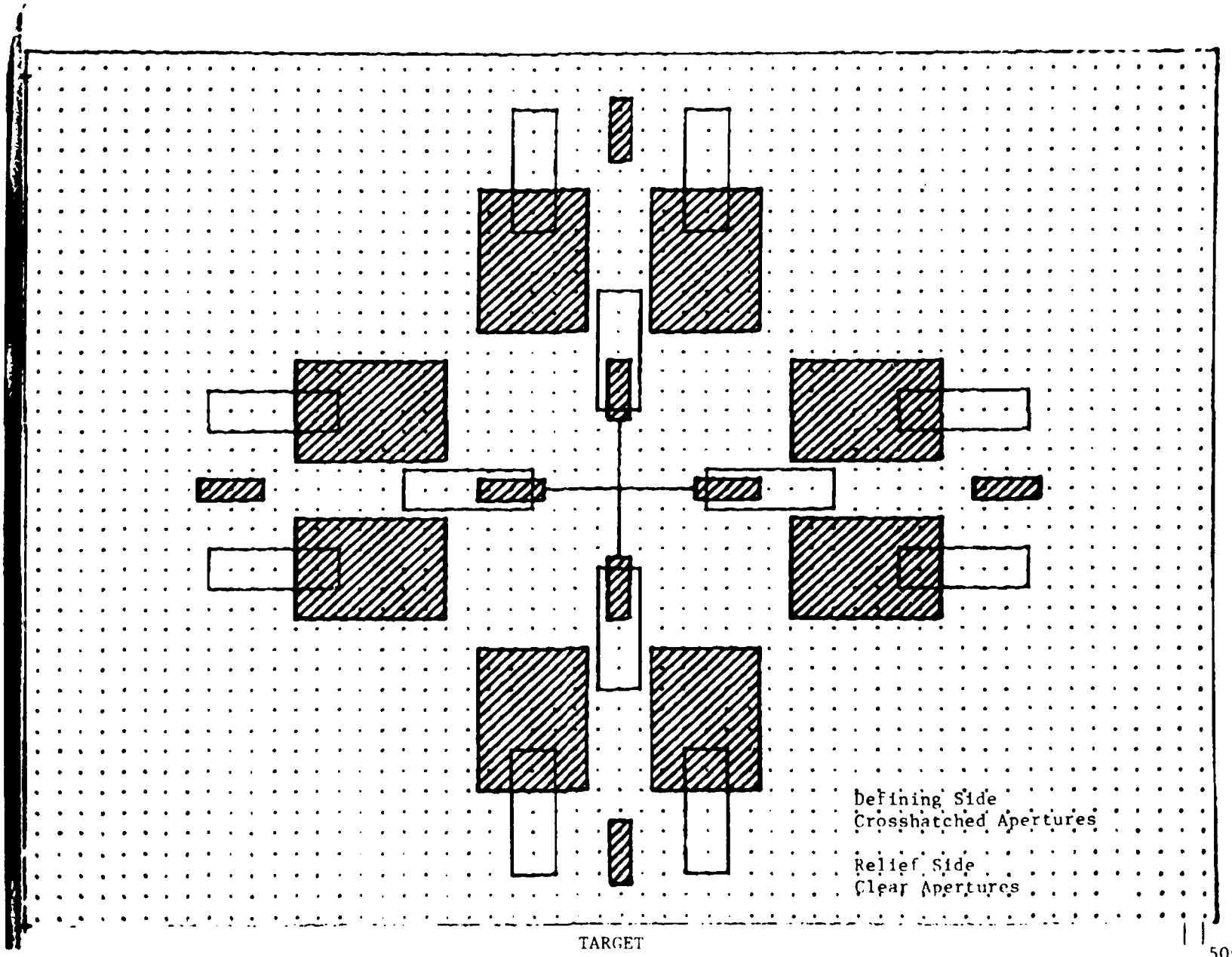


Figure 3.5. HIRES Memory Display

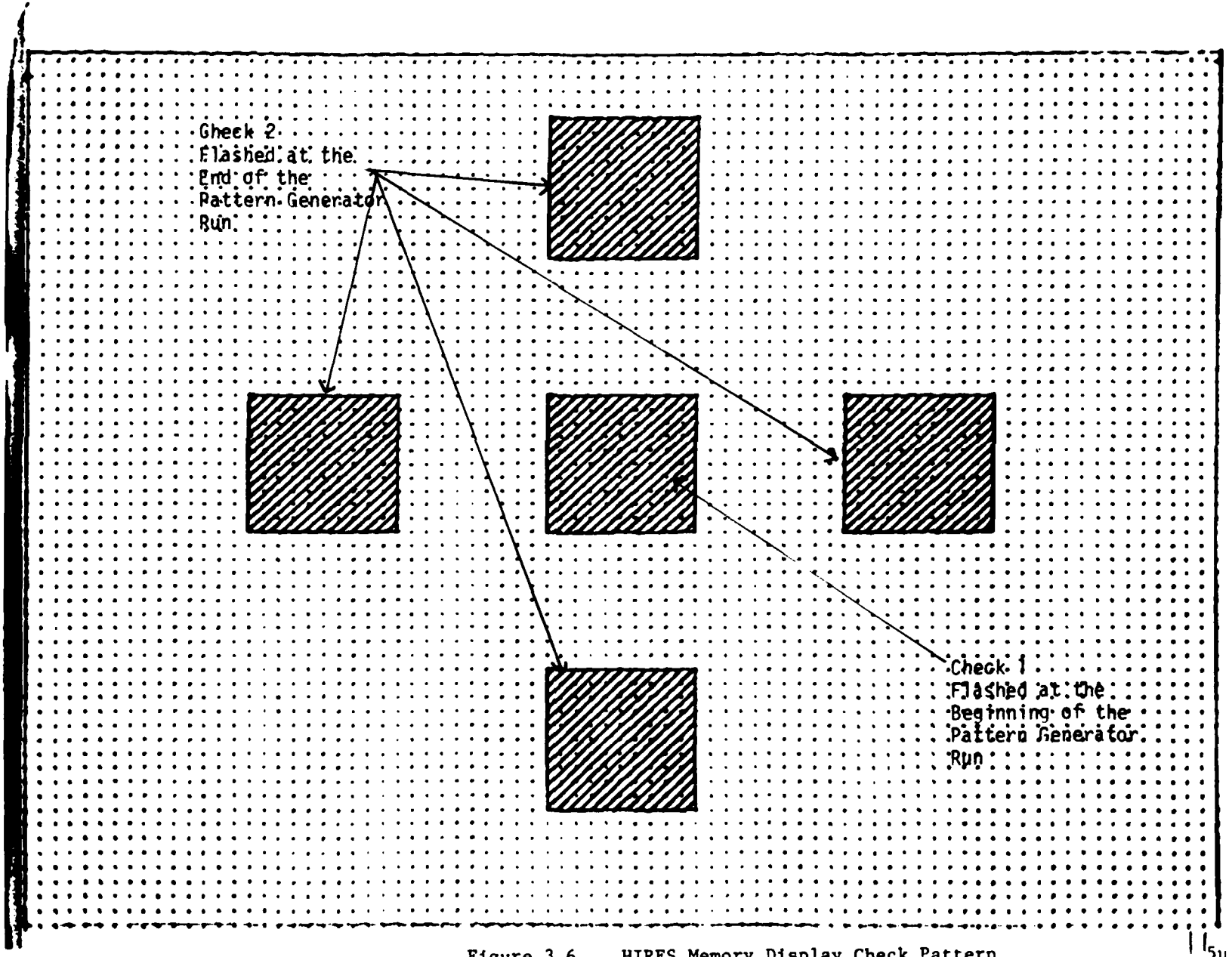


Figure 3.6 HIRES Memory Display Check Pattern

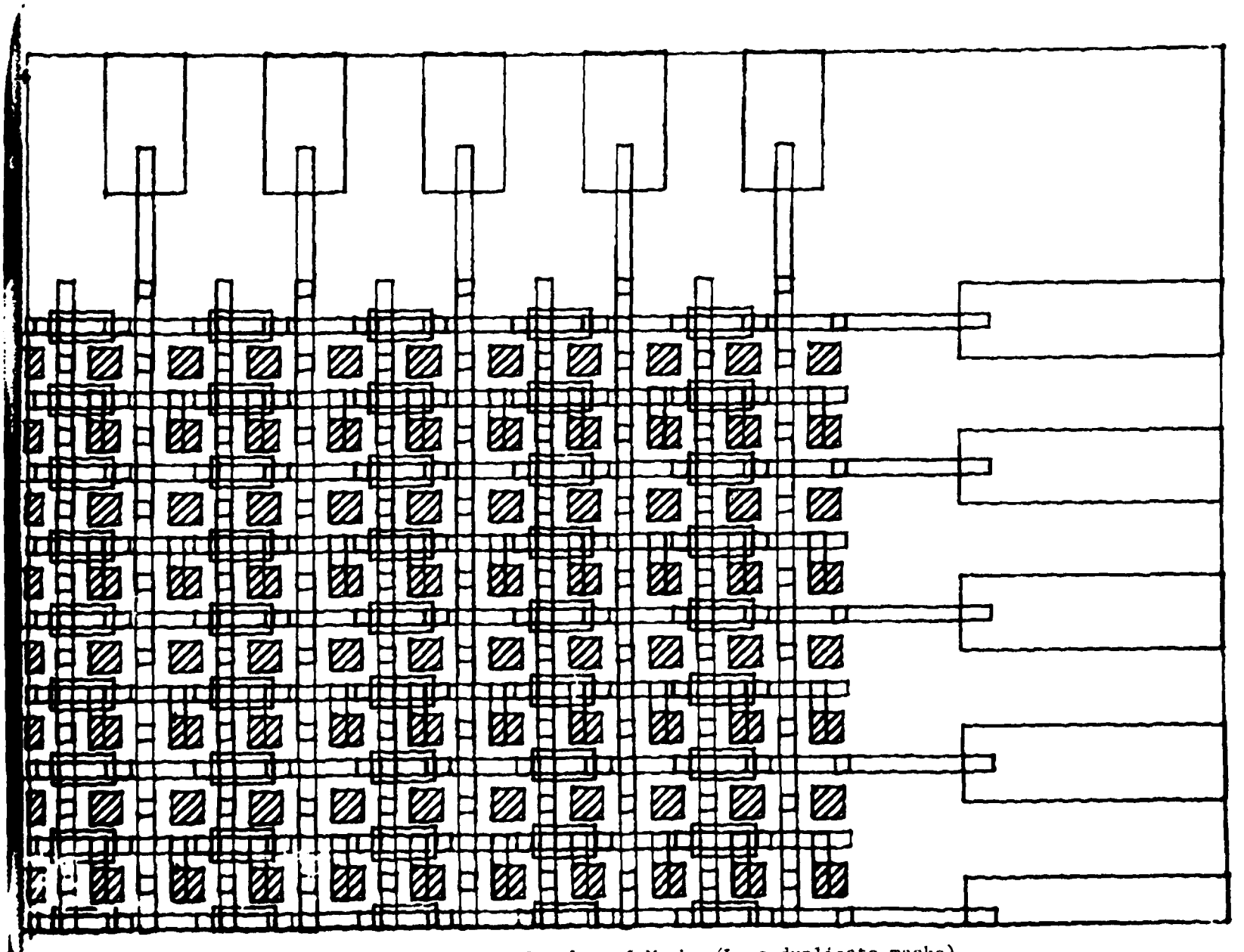


Figure 3.7 HIRES Memory Display Overlay of Masks (Less duplicate masks)

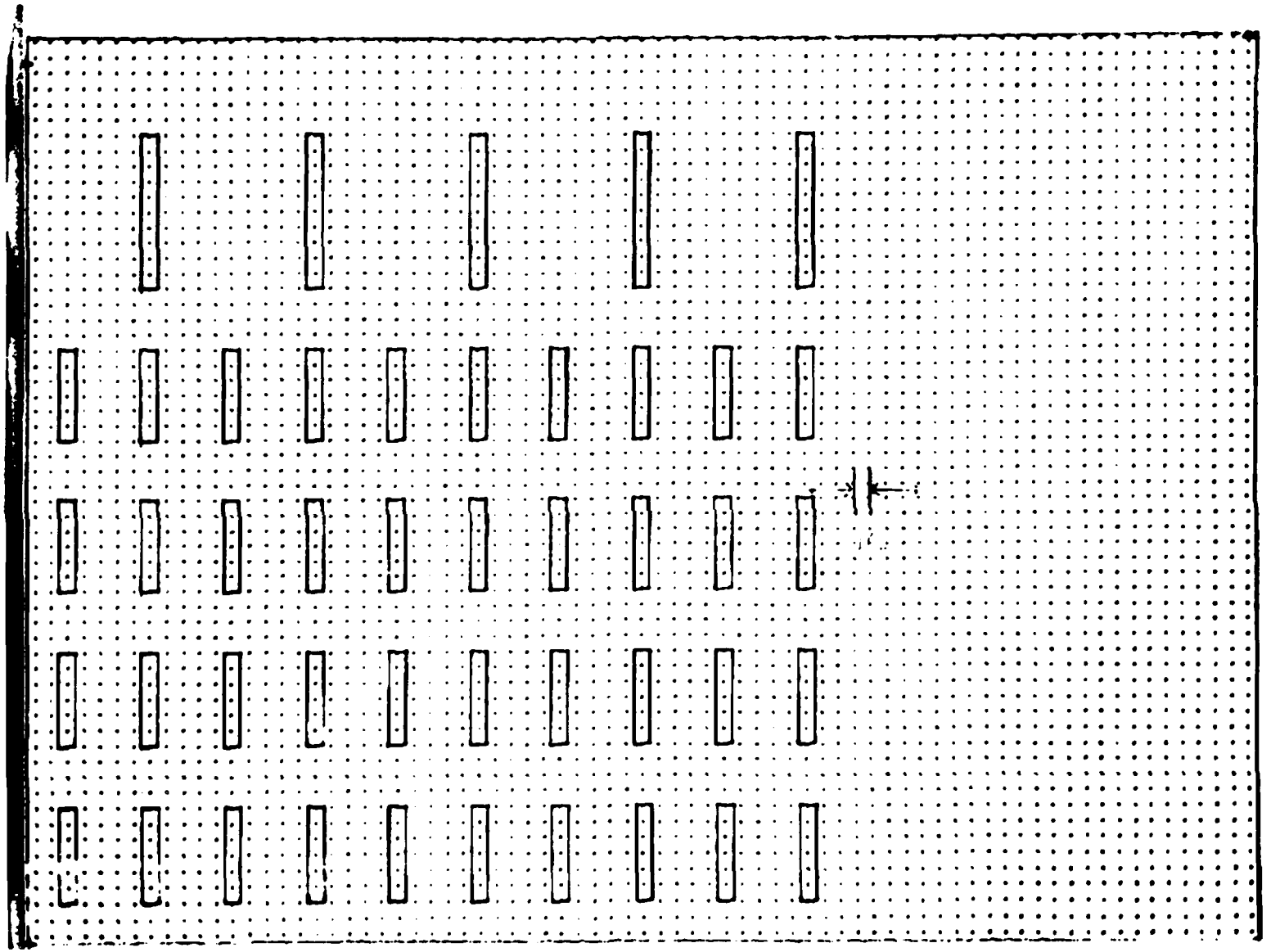


Figure 3.8 HIRES Memory Display
Mask #1 Vert IC #1 X Source

Defining Side Crosshatched
Finished Aperture Compensated 15μ/edge

Relief Side as Compensated

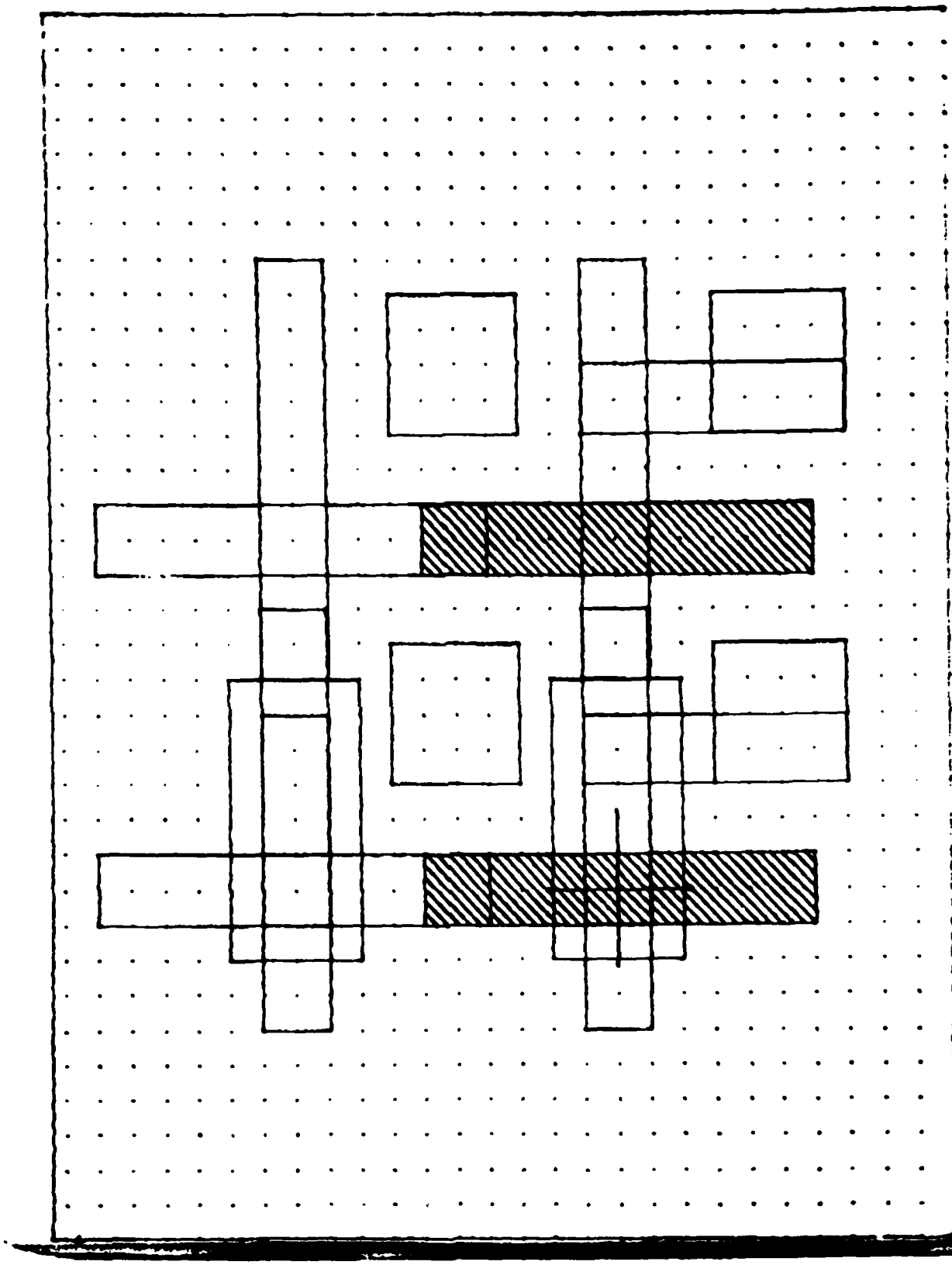


Figure 3.8(a) Location of Mask #1 in the Circuit

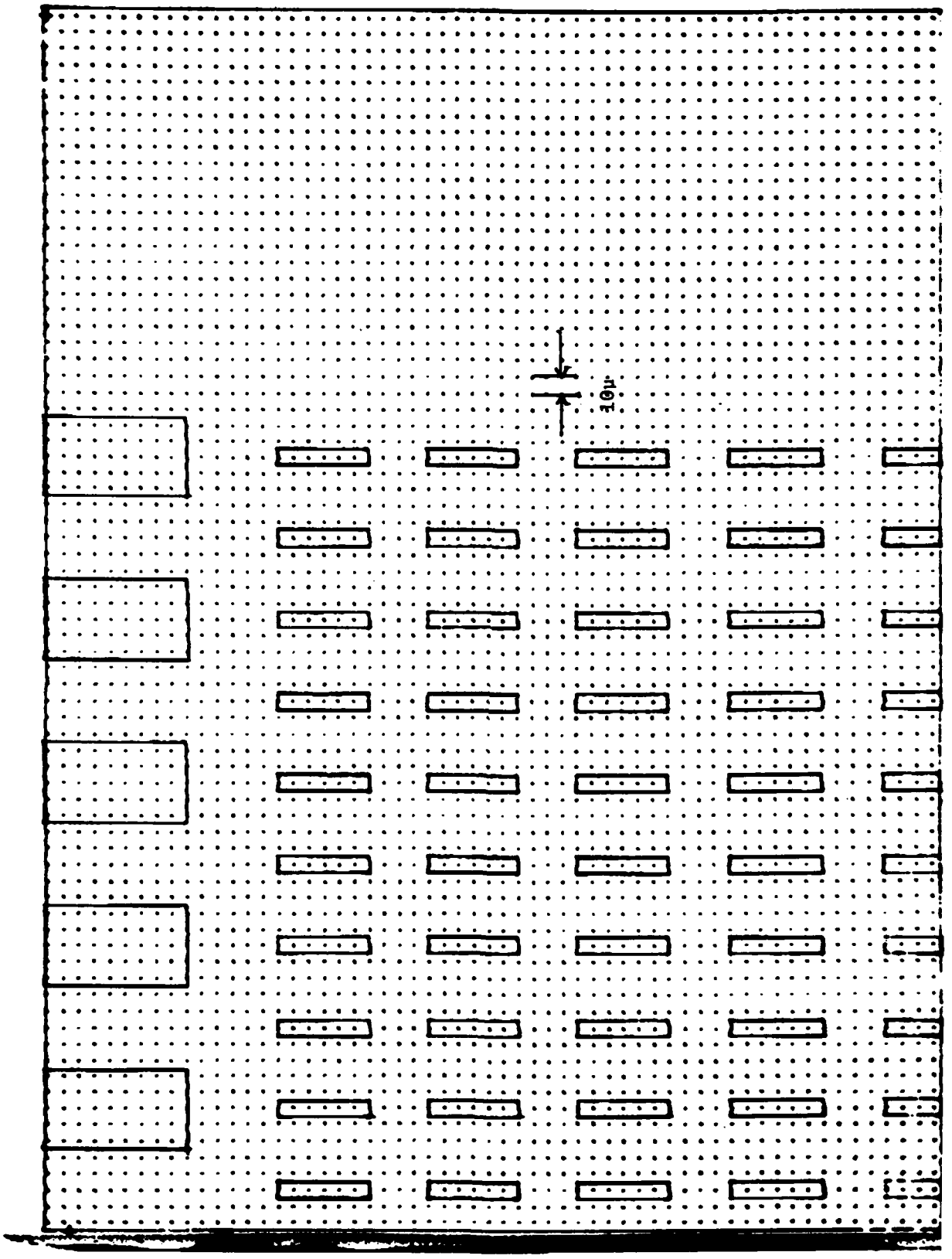


Figure 3.9 HIRES Memory Display
Mask #2 Vert IC #2 & Source

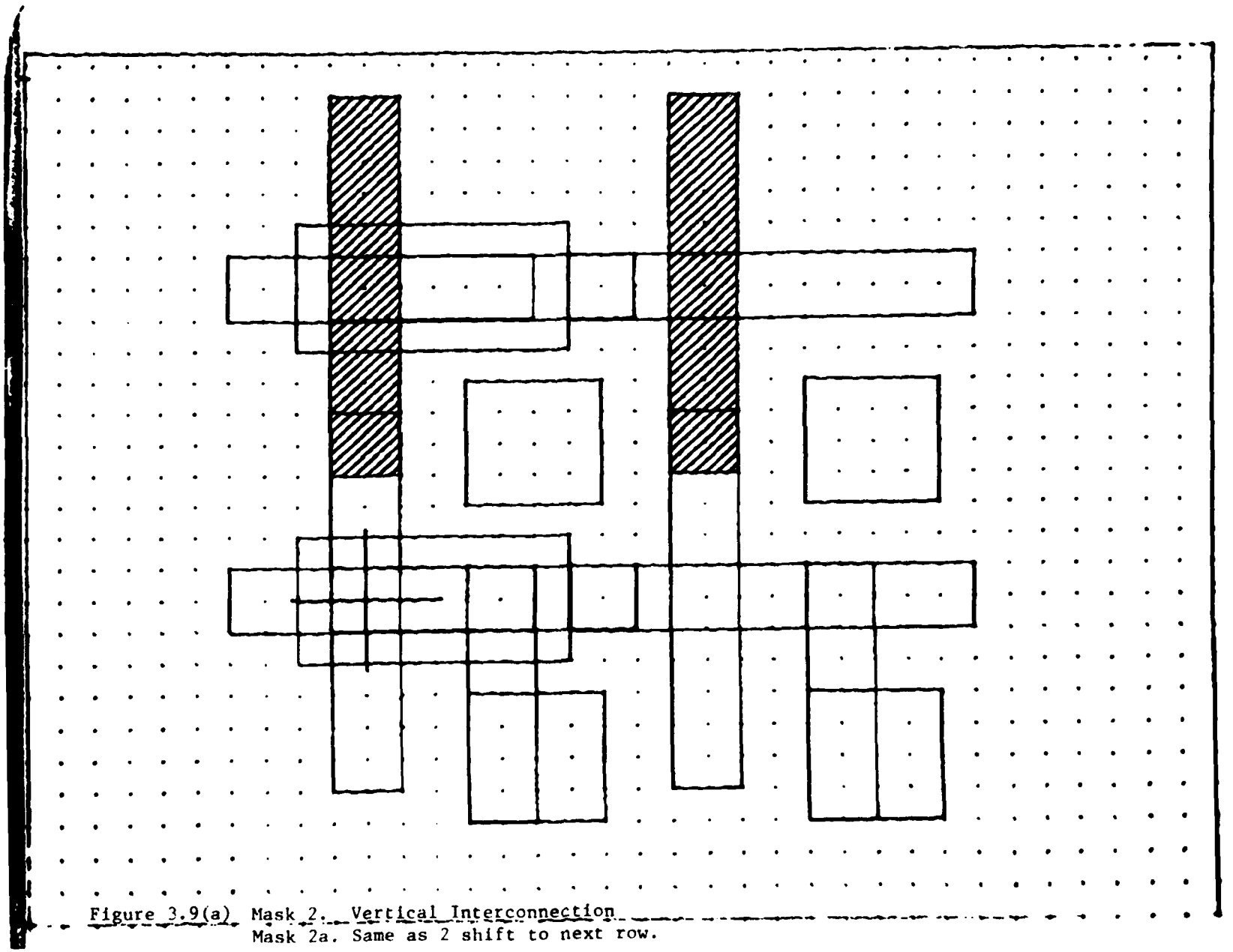


Figure 3.9(a) Mask 2. Vertical Interconnection
Mask 2a. Same as 2 shift to next row.

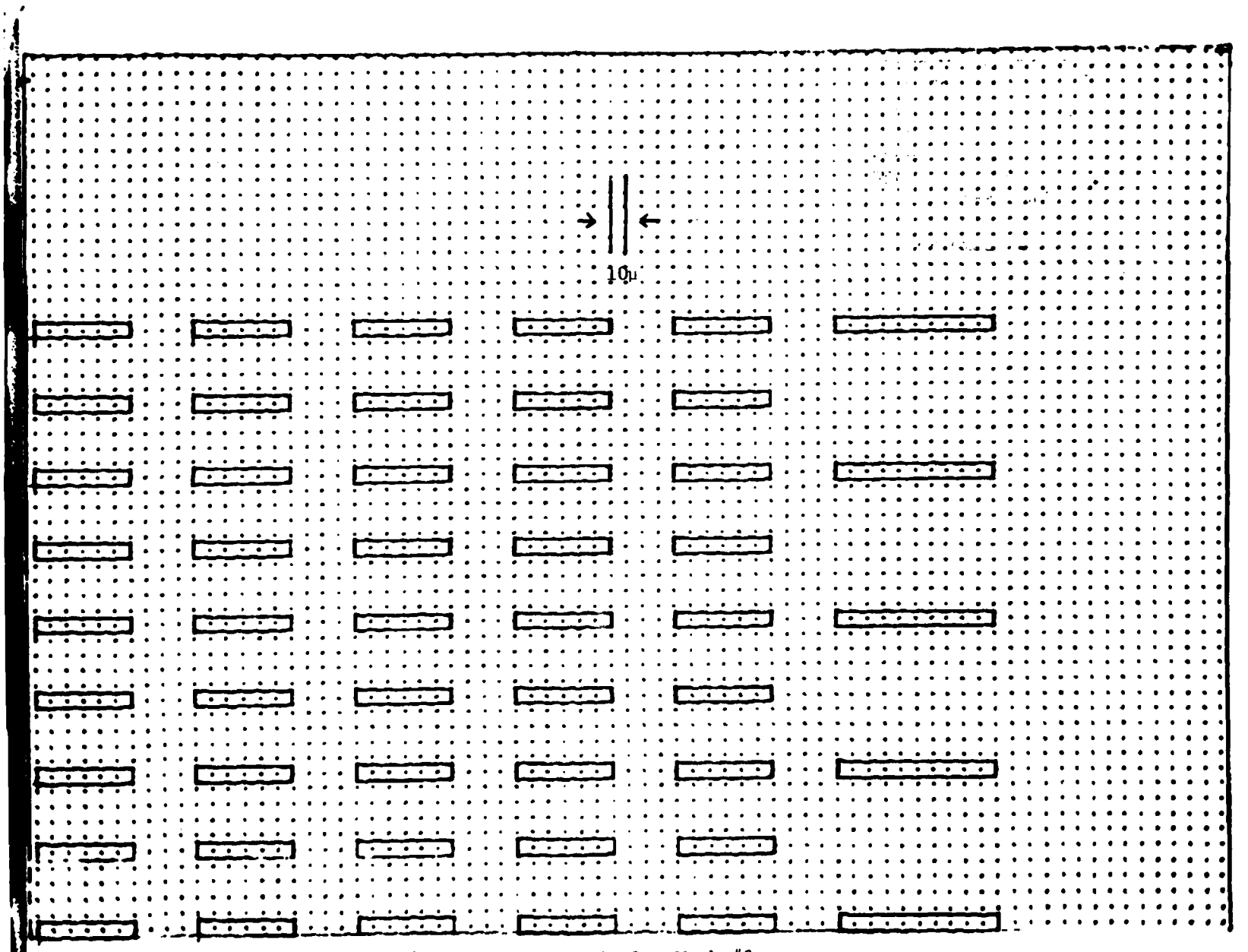


Figure 3.10 HIRES Memory Display Mask #3

Horizontal Interconnection #1 and
Gate

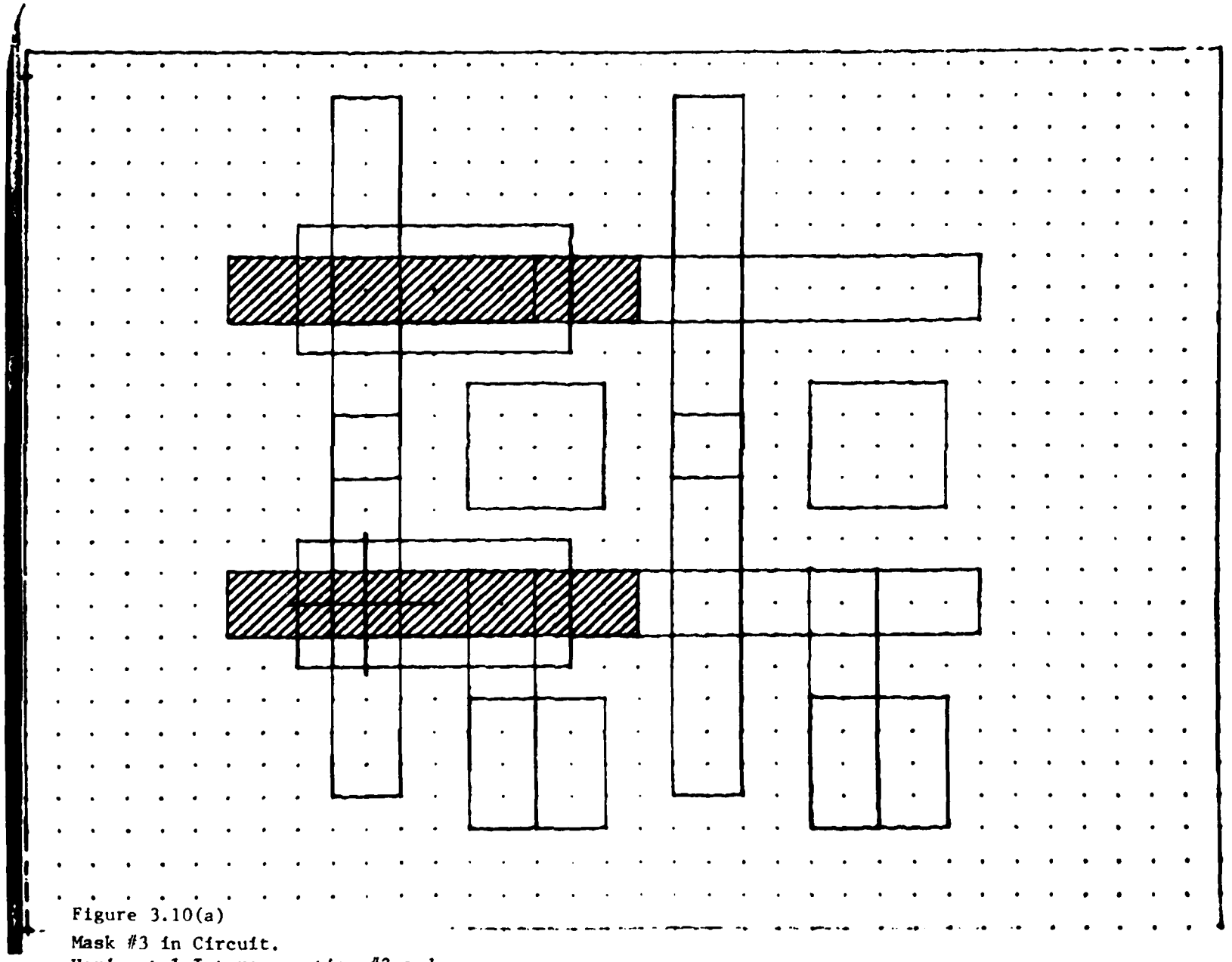


Figure 3.10(a)
Mask #3 in Circuit.
Horizontal Interconnection #2 and
Gate

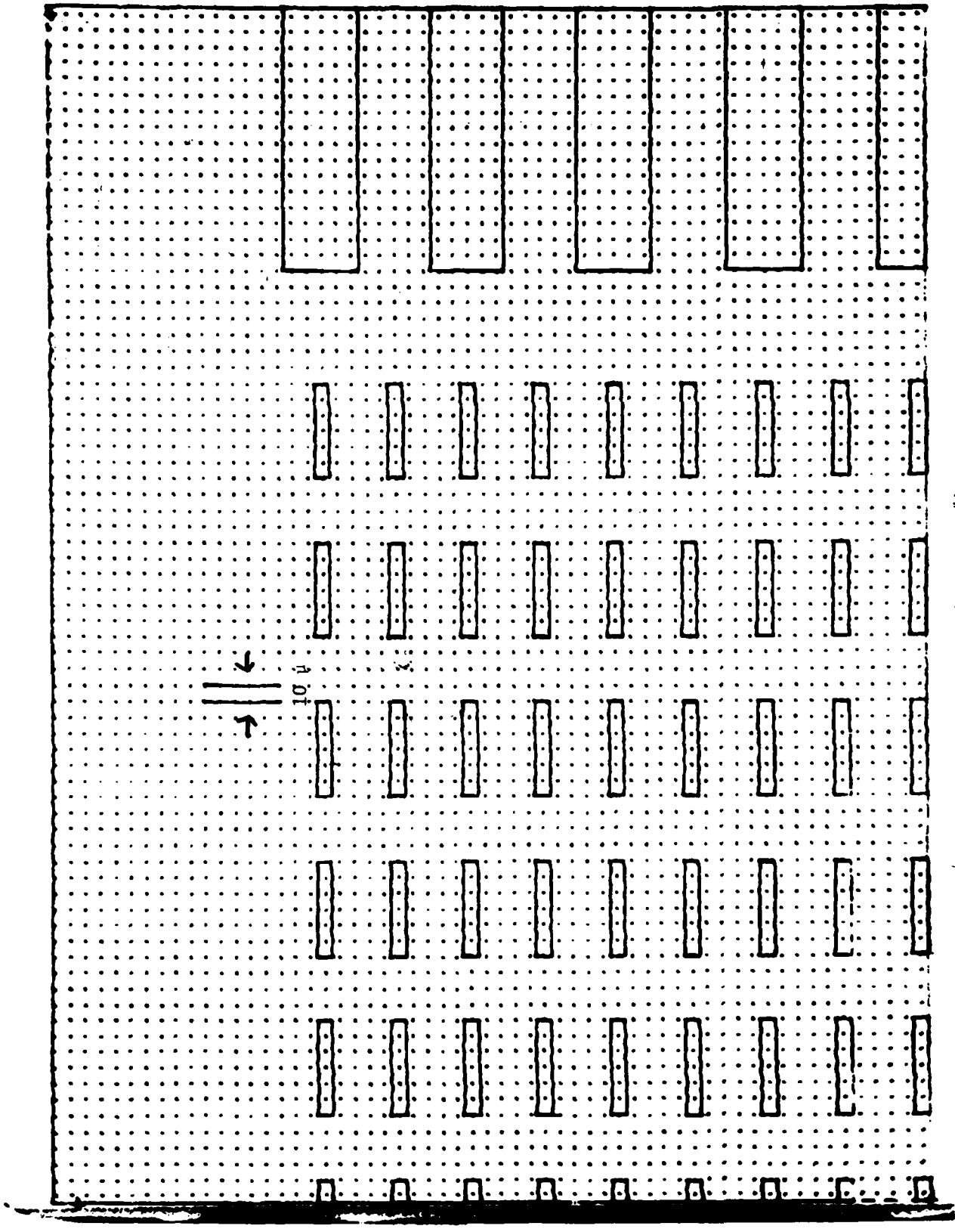


Figure 3.11. HIRES Memory Display Mask #4
Horizontal Interconnection and gate

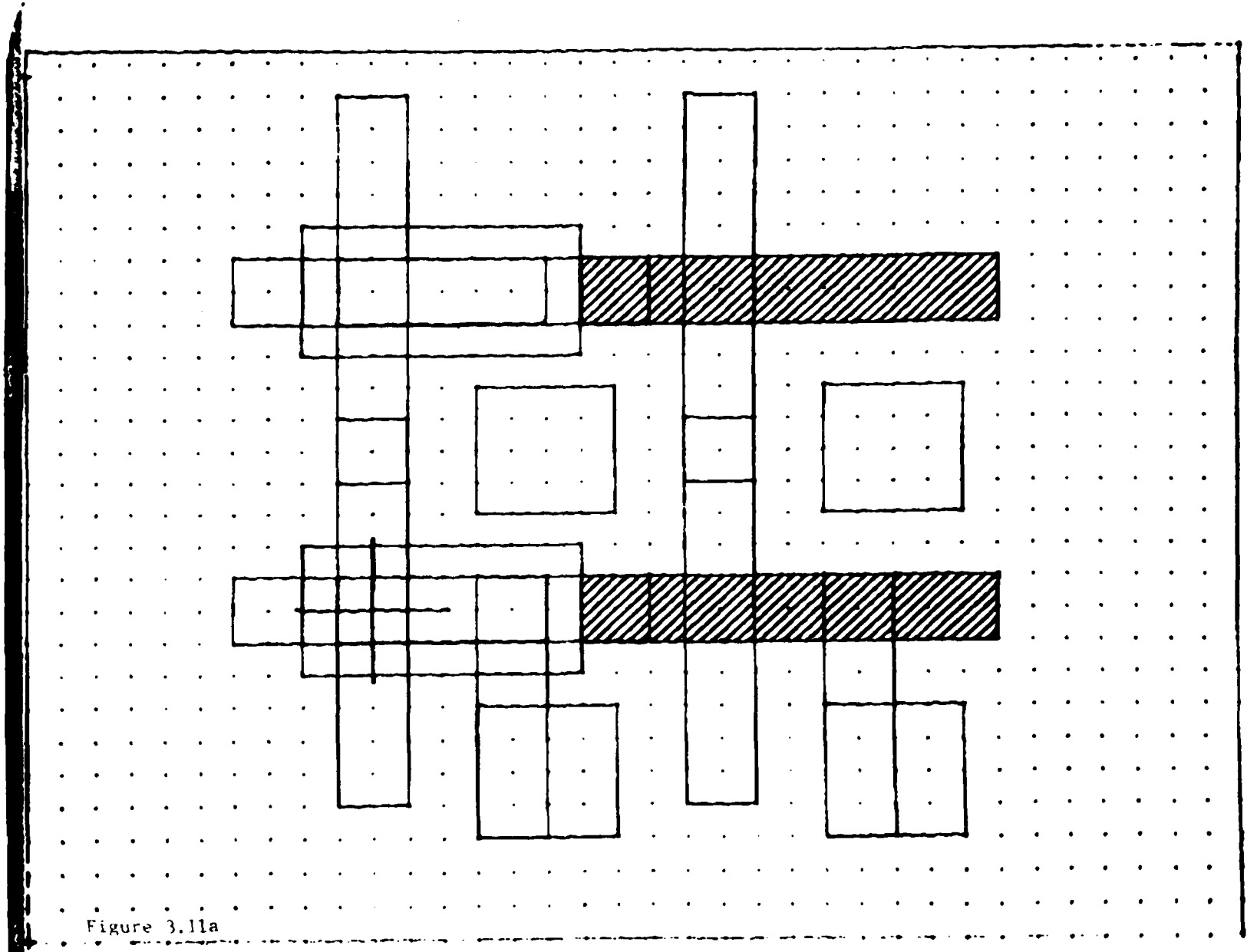


Figure 3.11a

Location of Mask 4 on circuit.
Horizontal Interconnection #1 and gate.

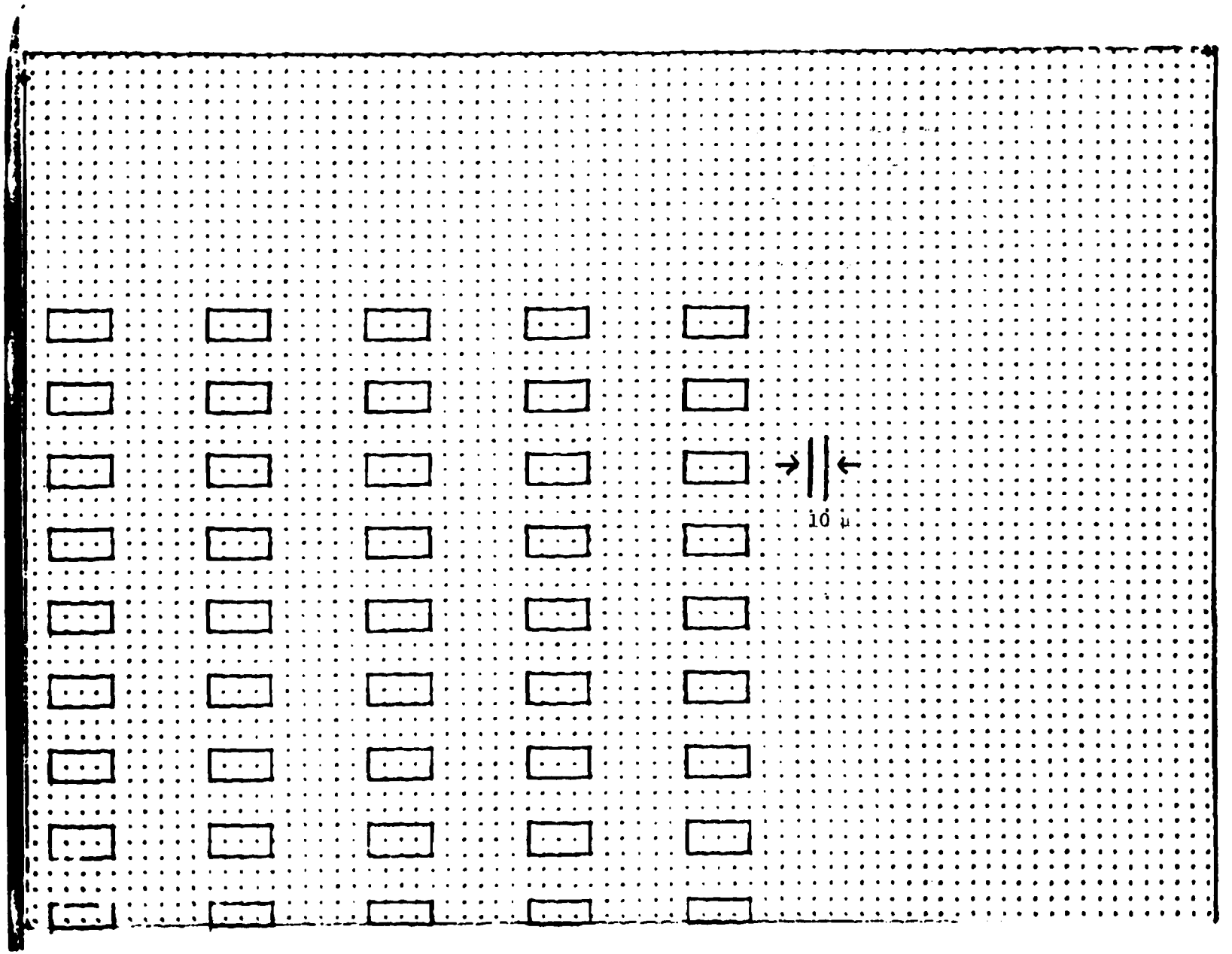


Figure 3.12. HIRES Memory Display Mask #5-6
Insulator #1 and #2

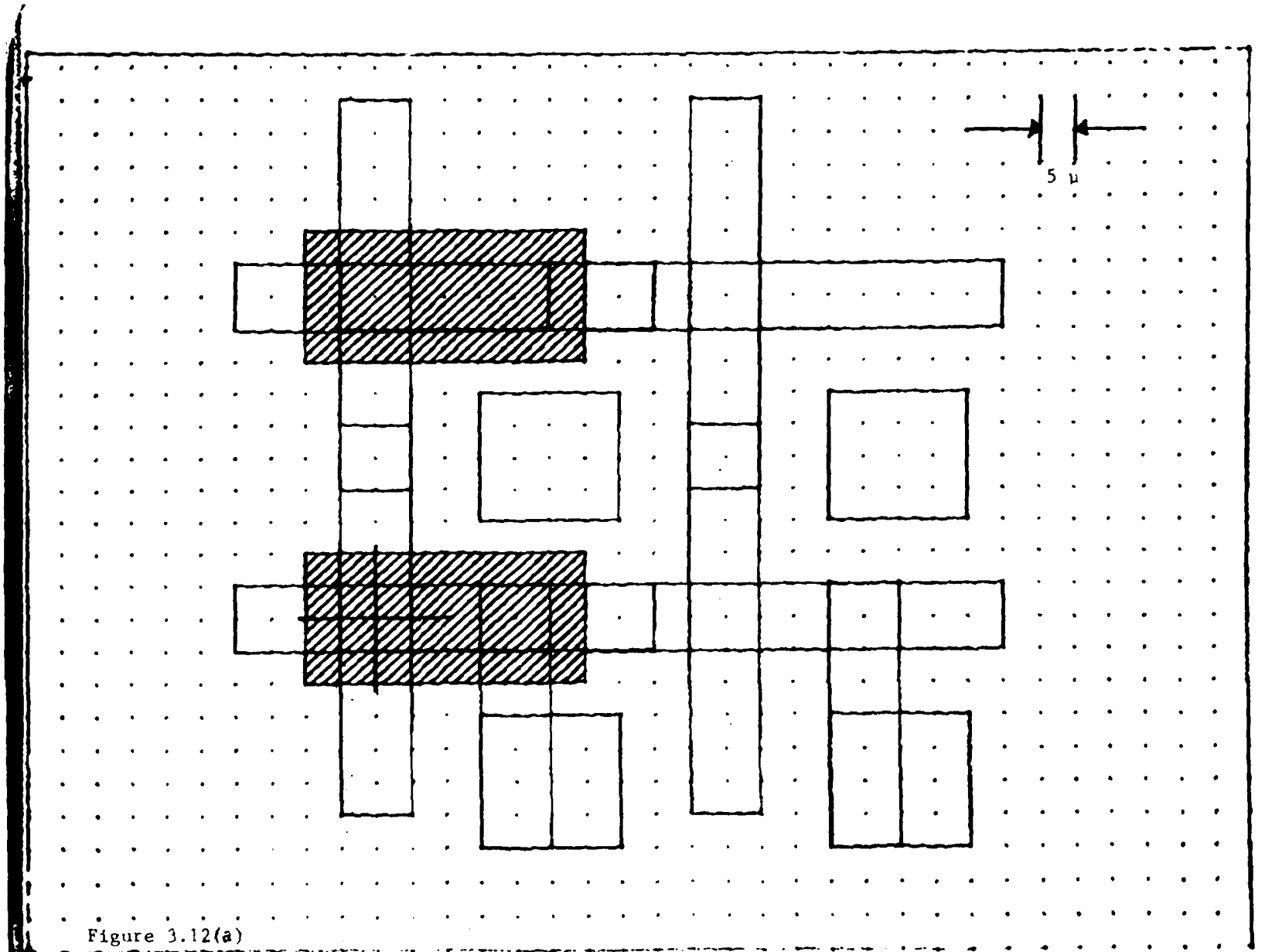


Figure 3.12(a)

Location of Mask 5 on circuit, Mask 6 is identical to Mask 5 but shifted to the next column.

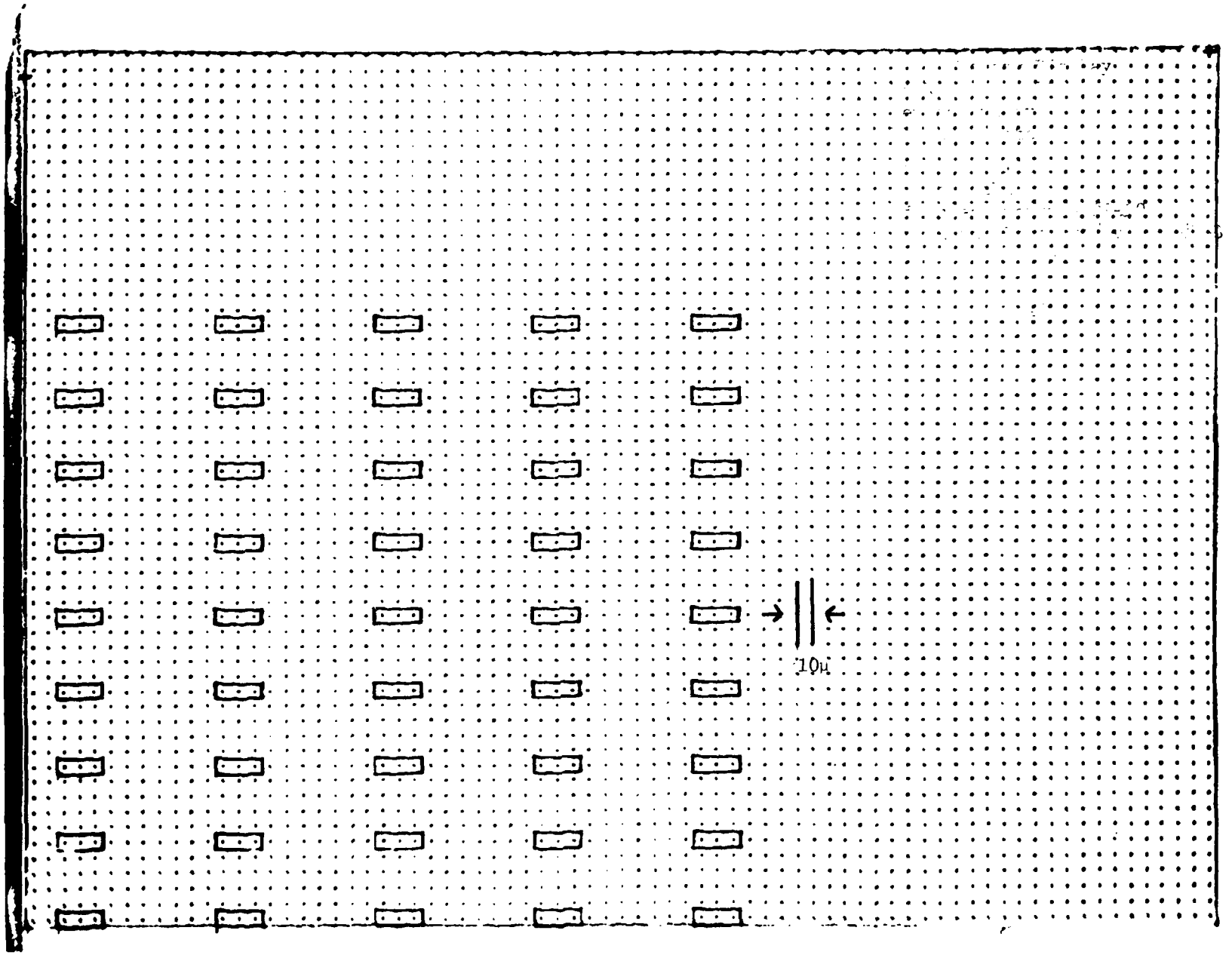


Figure 3.13 HIRES Memory Display Mask #7-8 #9-10
Semiconductor and Floating Gate

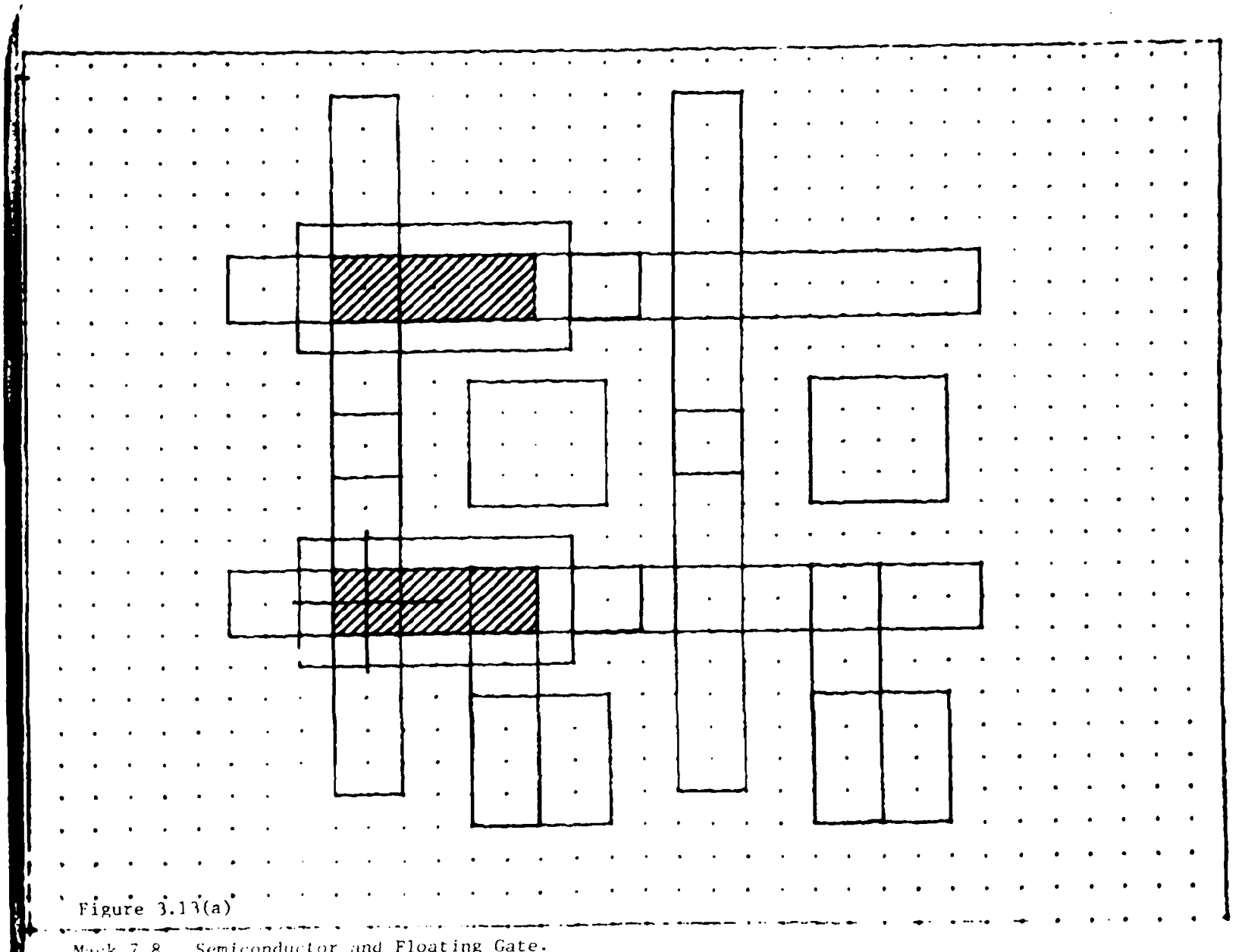


Figure 3.13(a)

Mask 7,8 Semiconductor and Floating Gate.
Mask 9,10 Same as (7,8) shifted to next column.

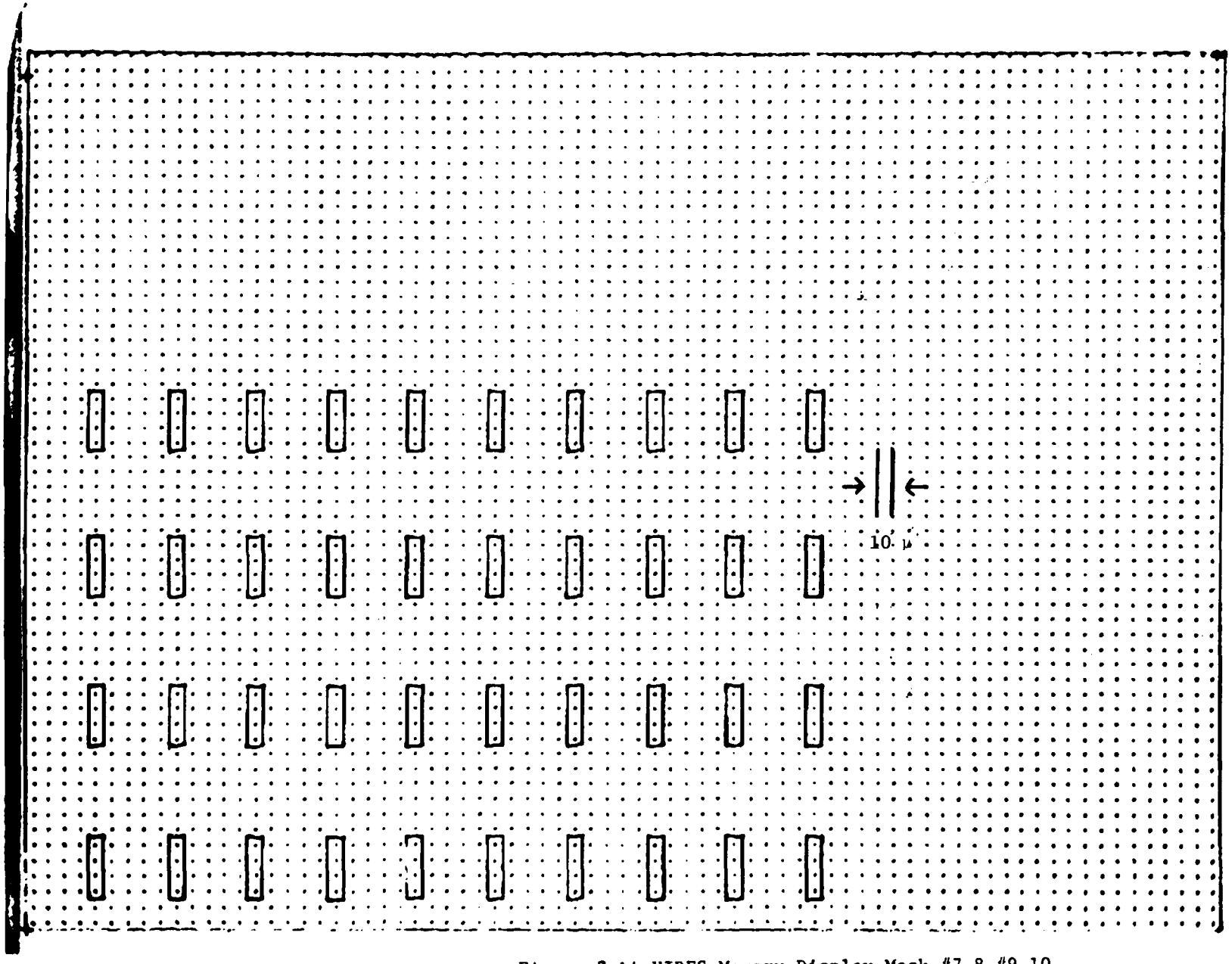


Figure 3.14 HIRES Memory Display Mask #7-8 #9-10
Transistor Drums

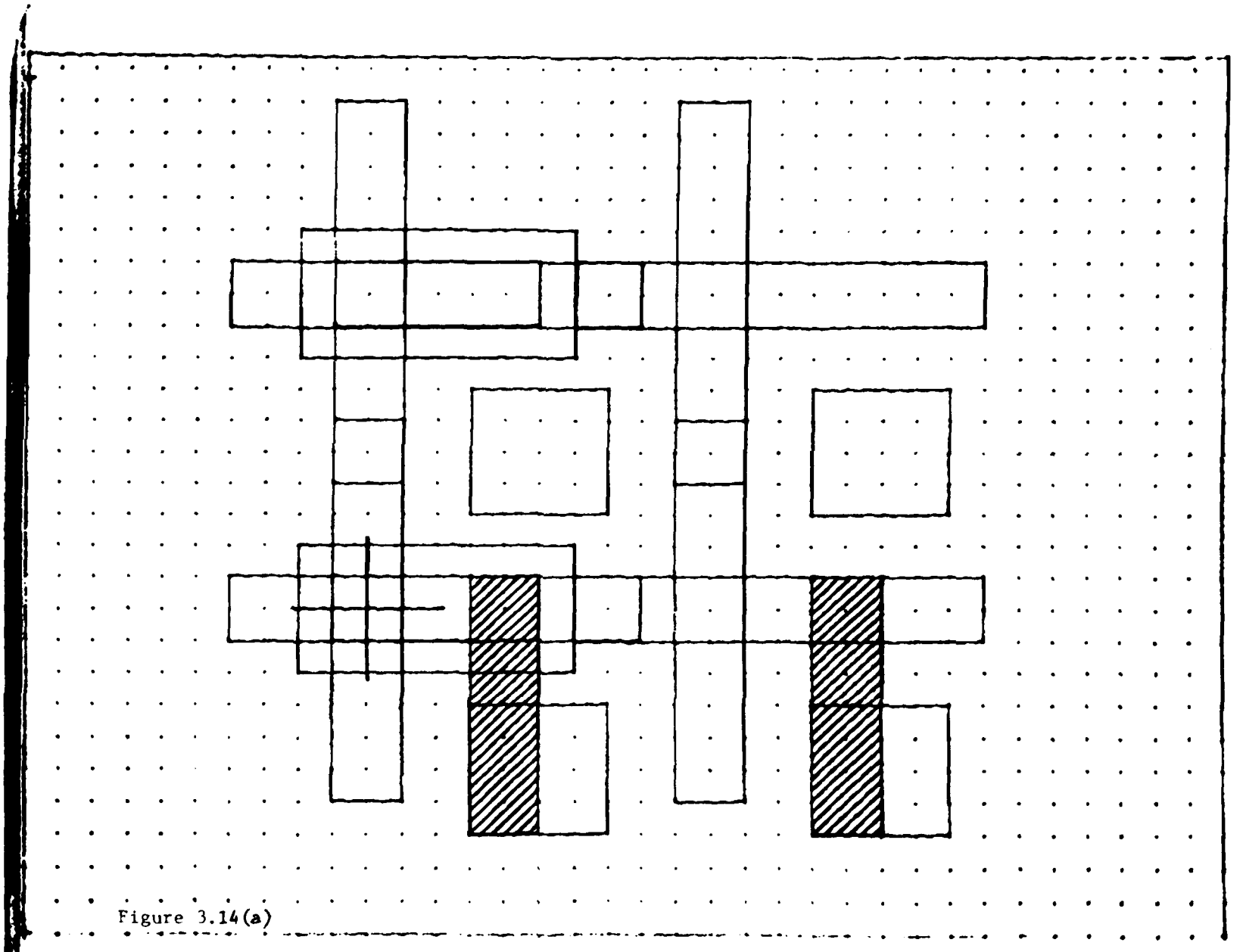


Figure 3.14(a)

Mask 11, Drain Mask
Mask 12, Same as Mask 11 shifted up one row

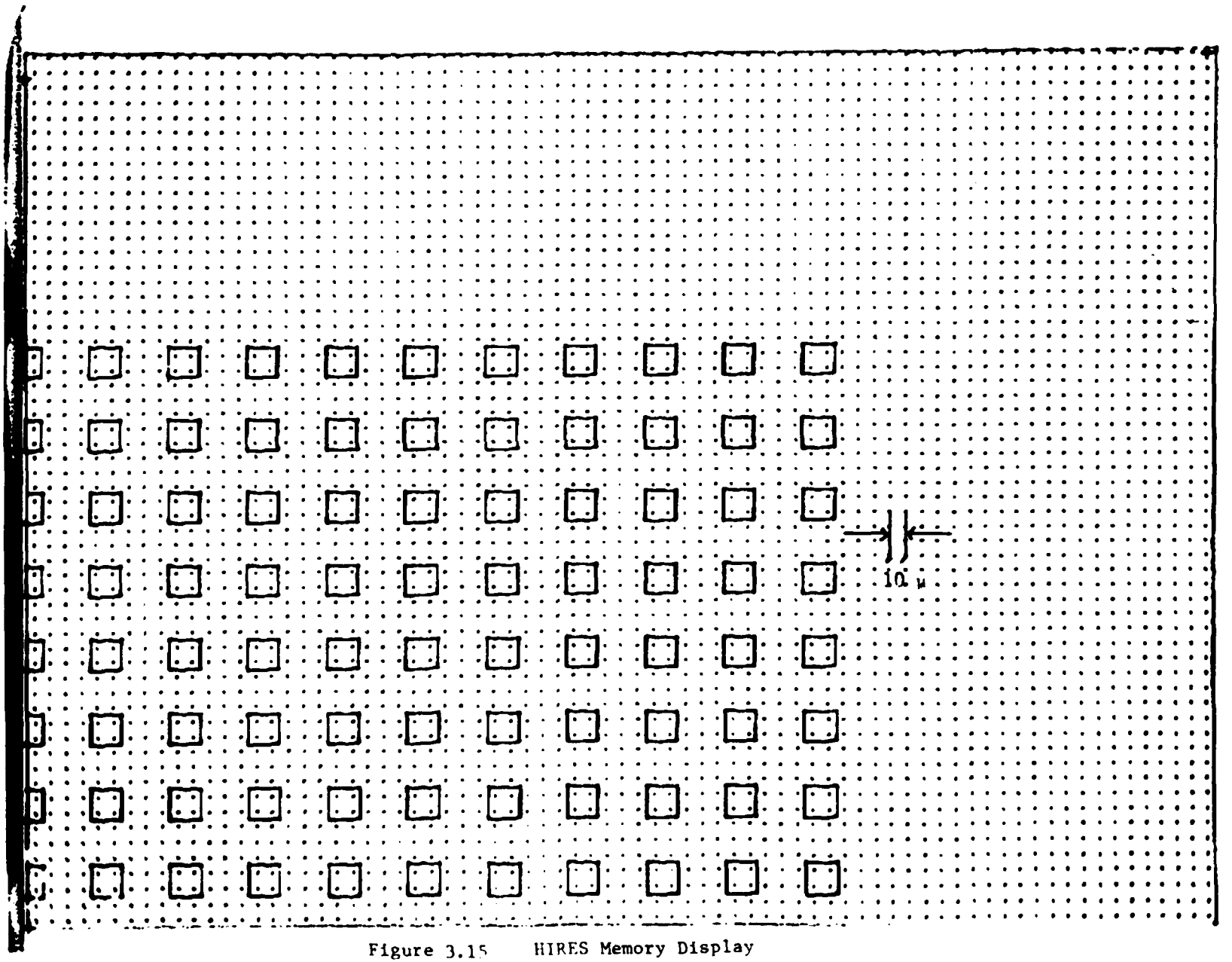


Figure 3.15 HIRES Memory Display

EL contact

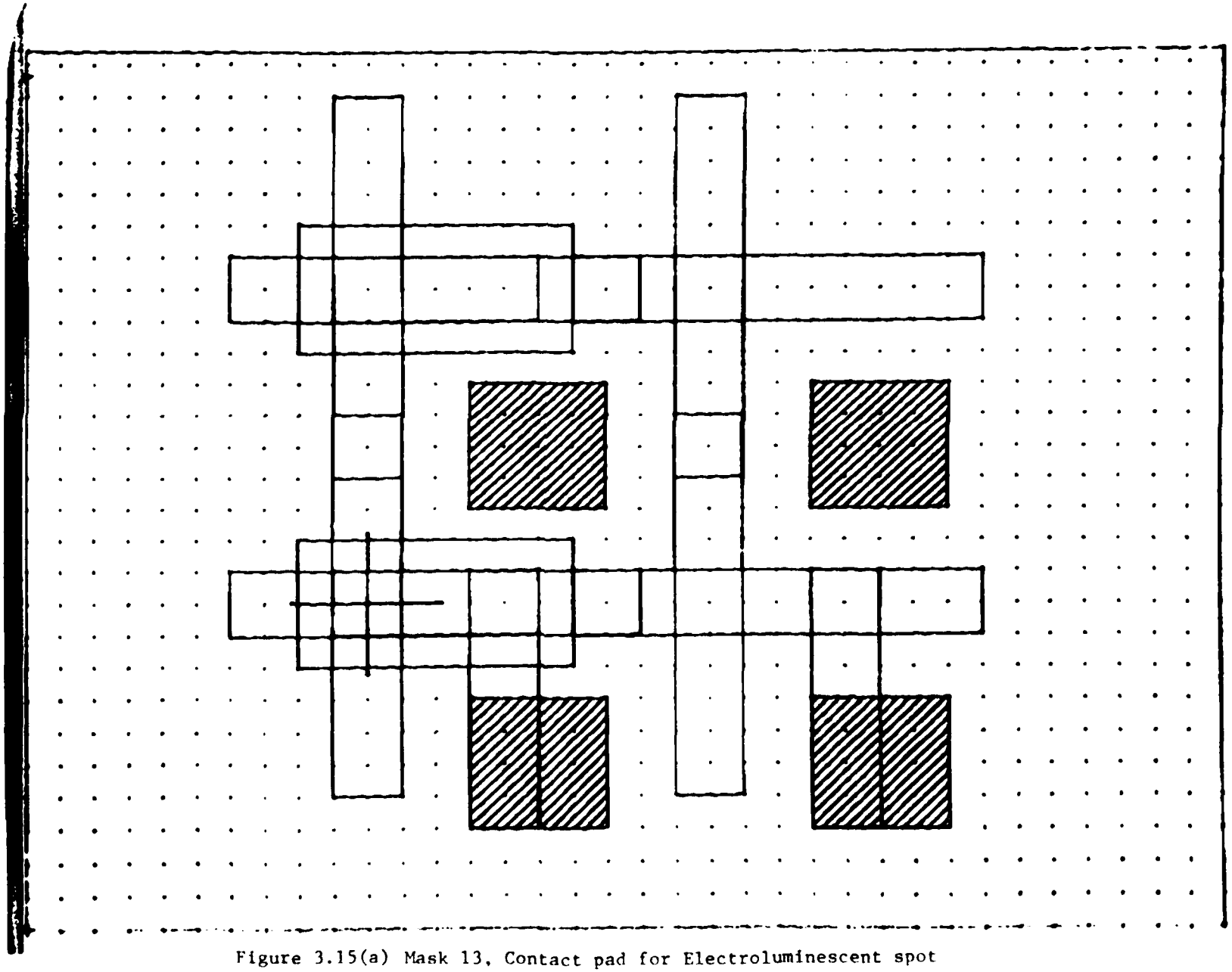


Figure 3.15(a) Mask 13, Contact pad for Electroluminescent spot

4. RESULTS

The time required for the production of the high resolution thin-film transistor display circuit was seriously underestimated. As a result of this, a working display at a high level was not produced. However, experiments were performed on the X-Y movable mask system and this section presents the results of these experiments as well as those of the alignment experiments which utilized a few of the series of dedicated masks that became available during the course of the contract.

4.1 X-Y Arrays

4.1.1 Aluminum Jig

In order to determine the capabilities of the X-Y mask system, a series of depositions using an X-Y jig made of aluminum, at a resolution of 128 x 128 per square inch, were made. Figure 4.1. shows a section of a panel at this resolution. By stepping one-half a unit in each dimension, a 256 x 256 array is made as discussed in Section 2. The jig is capable of accuracy to slightly better than .0005". The 256 x 256 array requires design dimensions of .0005" for deposition widths, overlaps and spacings, the performance of the jig is marginal. The achieved performance can be obtained only by allowing generous cool down periods after the alumina insulator depositions, which expose the equipment to prolonged radiant heating from the evaporant source. In one experiment, a 6 hour cool down between two sets of alumina depositions produced slightly over .0005" misalignment. Another experiment, involving a three-day cool down period, produced a shift slightly under .0005", which seems to be the capability of this equipment without the heating effect.

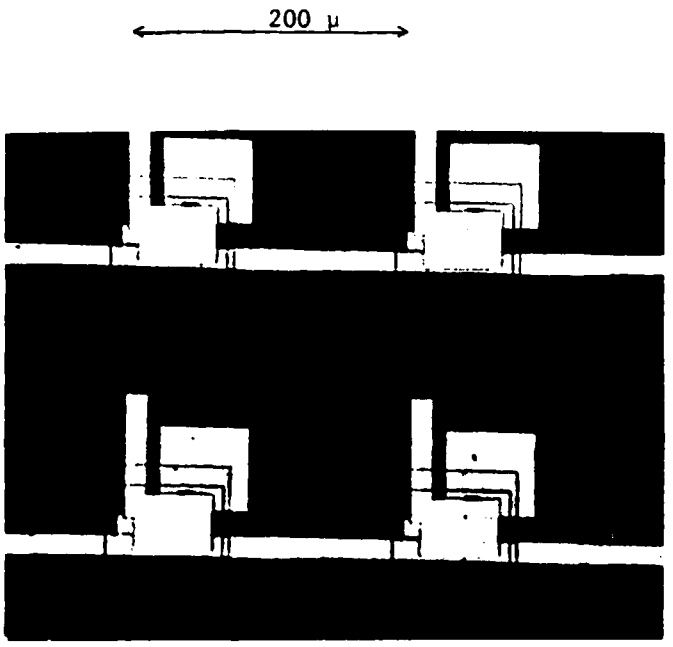


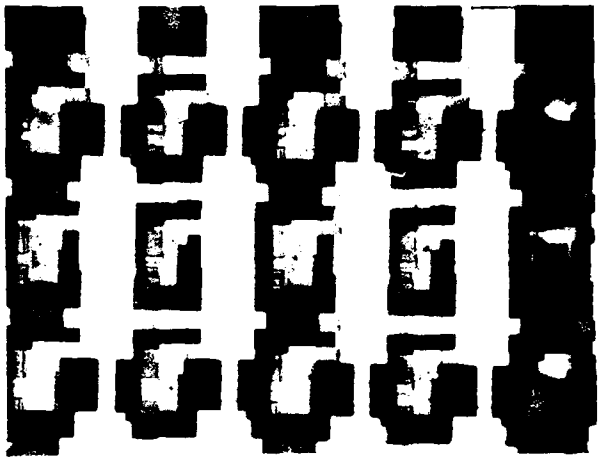
Figure 4.1

Photomicrograph of 128x128 Subarray

4.1.2 Tool Steel Jig

The tool steel jig which became available midway through the program proved to be better than the aluminum one. The two jigs differ in that the plates that slide over one another on ball bearings are made of aluminum in one case and tool steel in the other. Two separate attempts at a transistor array at the full 256 x 256 per square inch resolution are shown in Figures 4.2 and 4.3. As one can see from the figures, the alignments are quite good but still not good enough to assure good contacts over the whole circuit. Figure 4.4 shows transistor action measured on the substrate made just prior to the substrate shown in Figure 4.3. The substrate was not uniformly good over the whole surface.

Attempts to produce better alignments than those indicated in Figure 4.3 were unsuccessful and it was decided that we were operating at the reproducibility limit of the X-Y apparatus. The experiments done with the X-Y jigs led us to conclude that we should not pursue the acquisition of a pair of "repertoire masks" referred to in Section 2. A repertoire mask has all of the apertures for the circuit on one mask with a second mask used as a shutter to select the appropriate aperture. It had been our intention to purchase a high resolution set ($\gtrsim$ 400/ inch). However, it is clear that the rest of the apparatus (the X-Y jig) is only marginally capable of 256/inch resolution. Furthermore, since a major modification of the X-Y apparatus was not warranted (because of the short duration of the contract), we abandoned the X-Y approach at this point.



THIN FILM TRANSISTOR ARRAYS MADE WITH X-Y MOVABLE MASKS

128 APERTURES PER INCH MASK RESOLUTION

256 TRANSISTORS PER INCH ALONG X-Y

65,536 TRANSISTORS TOTAL

Figure 4.2

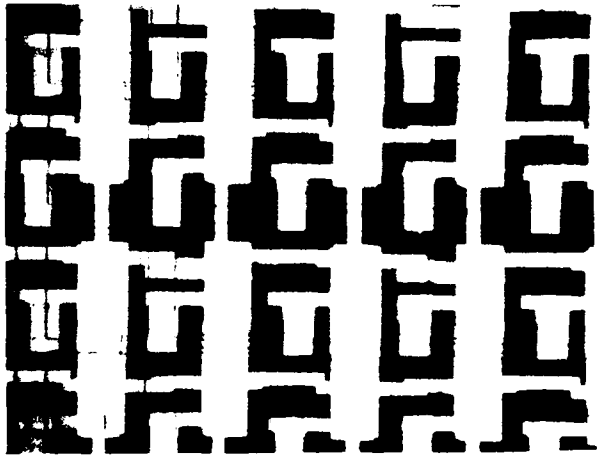


Figure 4.3

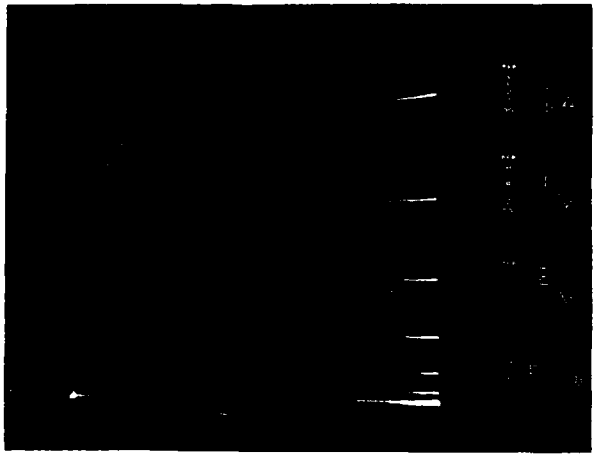


Figure 4.4

4.2 Dedicated Mask Program

Figure 4.5 shows a substrate holder with the mask holder and a set of dedicated masks that were used on an earlier project. The figure shows a substrate holder (at the top) which is lowered onto the mask holder and is aligned by means of two pins at each mask site that mate with holes in the substrate holder. The substrate holder also holds a strong ceramic magnet that pulls up on the mask in order to bring it into intimate contact with the glass substrate.

The dedicated masks described in Section 3 were ordered from Towne Labs in October 1977 and were delivered as they became available. The first two masks received were Mask #1 and Mask #3. Mask #3 is the reference mask to which all the other masks are aligned. It is used to deposit the horizontal interconnect lines which act as the gate electrodes for the memory transistors. The two masks are mounted on the mask wheel shown in Figure 4.5. Metal is deposited through Mask #3 the substrate is then shifted to Mask #1. Metal is then deposited through Mask #1. The pattern is examined and Mask #1 is adjusted on its holder and the evaporation sequence is repeated until the two masks are aligned satisfactorily. This procedure is repeated for each mask together with Mask #3. Figures 4.6. a and b shows the results of such an alignment run with Masks #1 and #3. The slight misalignment in the upper left corner of Figure 4.6(a).can be reduced by a slight translation of #1 (vertical lines) to the left, together with a small counter-clockwise rotation. The misalignment here is roughly 5 microns. The ability to make adjustments on this scale with screw down masks is limited to a great extent by the skill of the operator, and in this respect we face perhaps, a fundamental limitation of the method.

With the receipt of Masks #2, 4 and 5, we were able to make trial depositions with the combinations of the five masks #1 through #5. All masks were aligned with respect to Mask #3 as discussed above prior to the depositions shown in Figure 4.7. Figure 4.7 is as indicated earlier a composite picture of the areas on a one inch

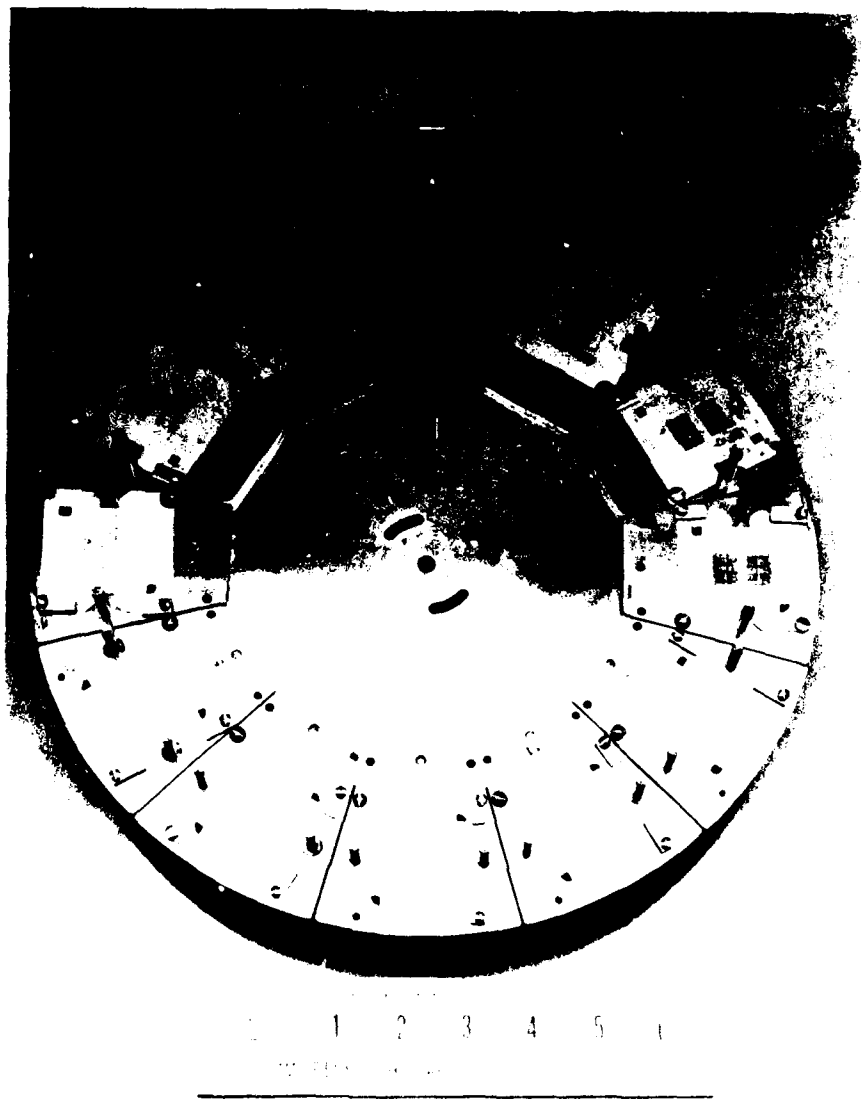


Figure 4.5. Mask and substrate holder for the dedicated aperture masks. The masks shown here were used on a previous program.

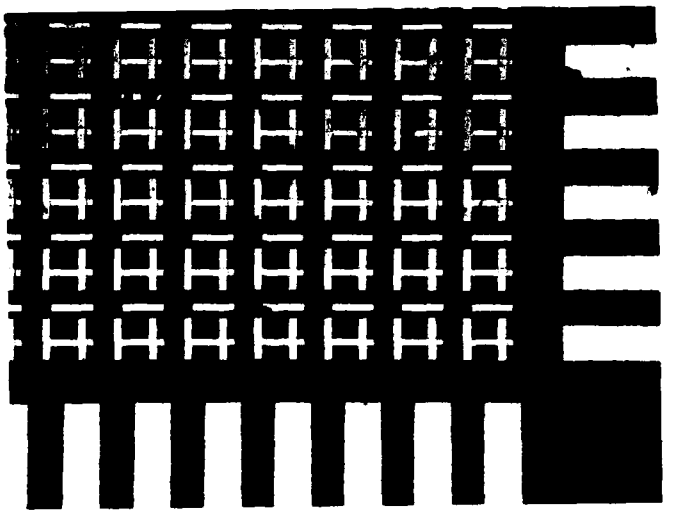


Figure 4.6(a)

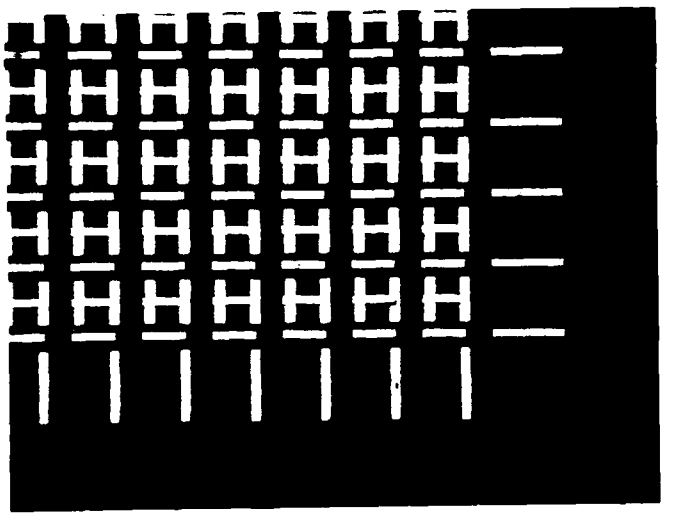


Figure 4.6(b)
Evaporation Through Aperture Masks #1 and 3

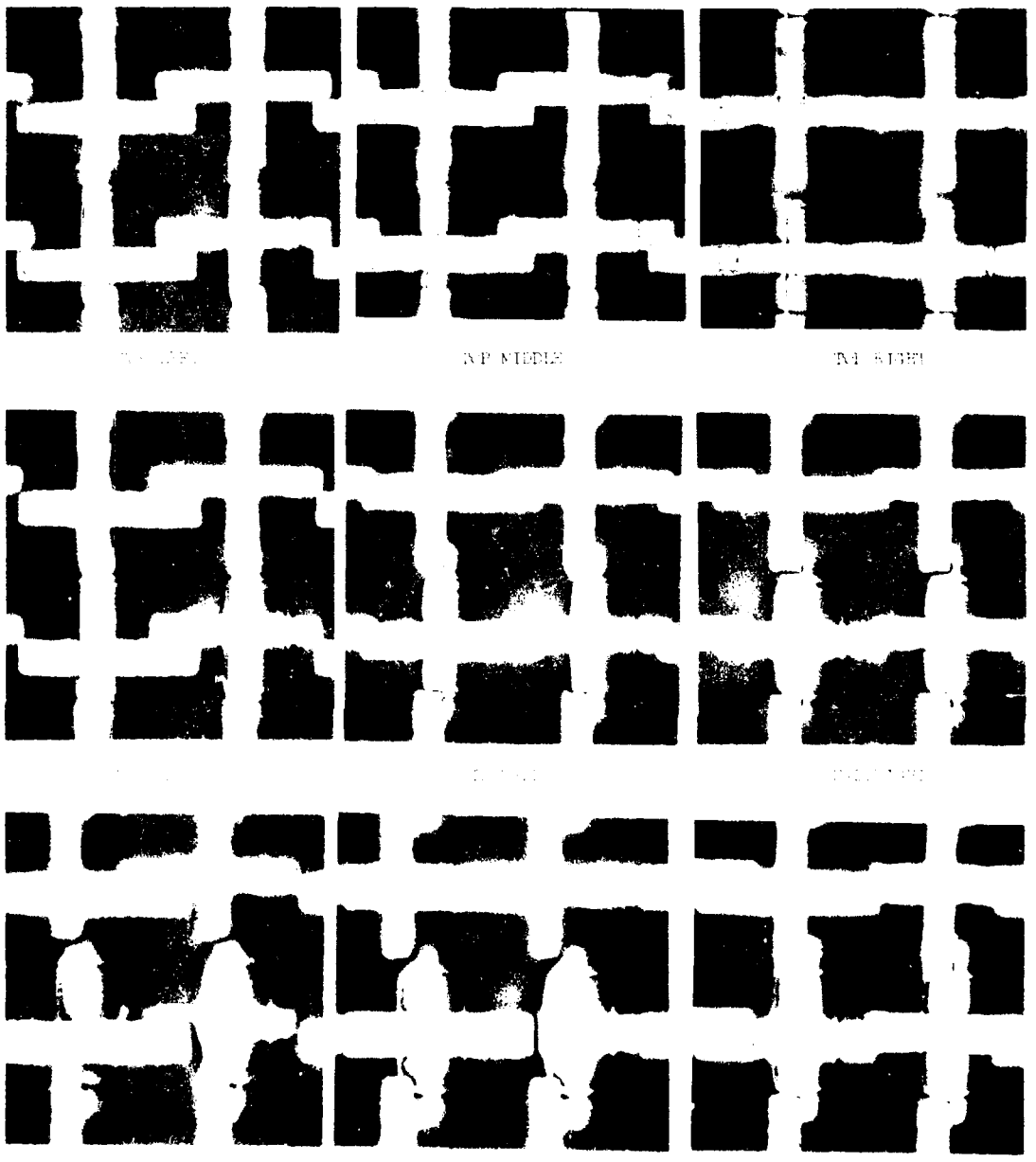


Figure 4.7 Trial Deposition, Masks 1, 2, 3, 4, and 5 (600X)
Miniature Active Matrix Display

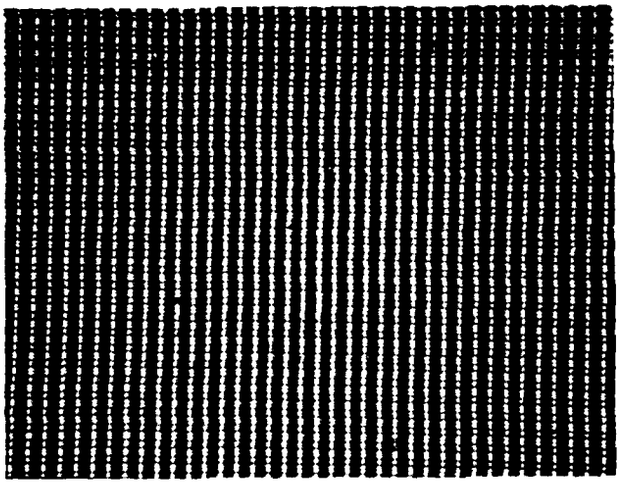


Figure 4.8

500 lines/inch x-y conductors on thin film electroluminescent sandwich

(Y_2O_3 - ZnS:Mn - Y_2O_3)

Bottom conductor: NESATRON
Top conductor: Aluminum
Magnification: X60

Figure 4.9

Same as Fig. 1

Magnification: X250

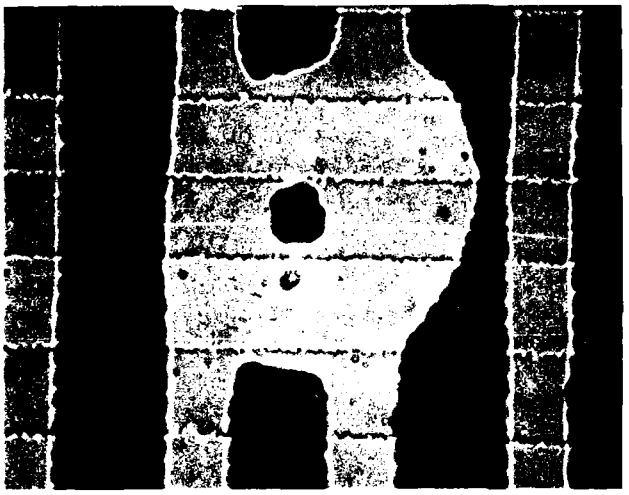


Figure 4.10
Short caused by imperfection in the photomask

Figure 4.11

Damage caused by etching the top electrode in a mixture of phosphoric and nitric acids.

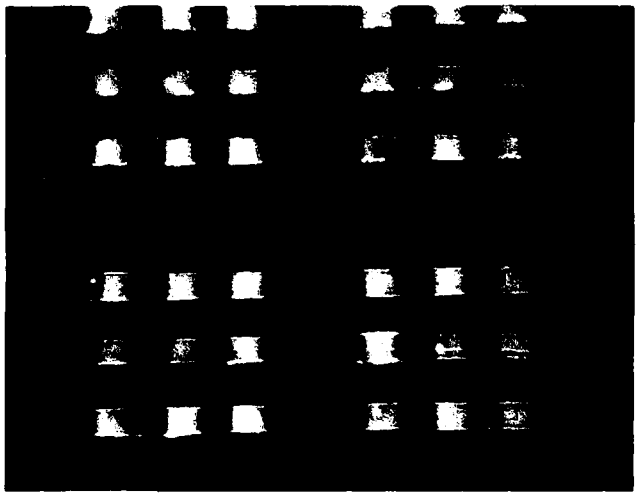


Figure 4.12
Addressed elements showing 500 lines/inch resolution and high contrast.

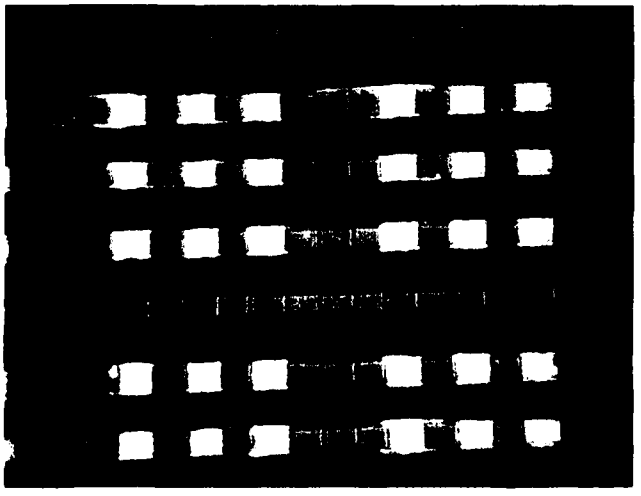


Figure 4.13
Addressed elements with ambient light added to show location of illuminated areas.

Figure 4.14 Sample high resolution element made with powdered phosphor (ZnS) and with continuous electrodes top and bottom. To make the lines, SiO_2 was evaporated over the bottom electrode and etched to leave holes. The phosphor was sprayed over the SiO_2 and covered with gold. The extra thickness of dielectric between the squares keeps those regions dark. Photo taken with phosphor lit.

substrate. Misalignments of the order of 10 μm are evident in the bottom-middle section of the figure. The cause of the misalignment may be thermal expansion or inadequate mask pullup by the magnet behind the substrate. The fuzziness of the insulator on the bottom suggests that mask pullup may be the likely cause.

The delay in delivery of masks was due in large part to the long run times on the Mann pattern generator that produces the photomasks from which metal masks are made. The run times were reduced to 17 hours by sorting out the flashing sequences so as to reduce the dead time between flashes. Such long run times had to be scheduled ahead of time and resulted in long delays because of the work load on the machine. As a result, the full set of aperture masks were not delivered until well after the scheduled end of the program.

4.3. Passive Panel

While waiting for the delivery of the high resolution dedicated masks, experiments were conducted to determine a suitable display medium to use in conjunction with the display circuit. The display media tested were:

1. Thin film electroluminescence
2. Powered electroluminescence

The thin film electroluminescent structure consists of a layer of manganese doped zinc sulfide sandwiched between two layers of a high dielectric constant, high strength insulator (e.g. Y_2O_3). The first layer of Y_2O_3 is electron beam evaporated onto a NESA(R) coated substrate that has been etched to leave parallel bus bars at 500 lines/inch resolution. An aluminum electrode is deposited on top of the last Y_2O_3 layer and etched with the same bar pattern at right angles to the first. An ac voltage applied between a horizontal and a vertical bus bar will excite the film to luminescence when the voltage exceeds a threshold value. The steepness of the brightness voltage

characteristic of the EL allows the individual addressing of the elements at the intersections without cross talk. Figures 4.8 through 4.11 show the passive structure with defects of various kinds resulting from photomask defects and etching damage. More time and greater care could perfect this type of passive display at 500 lines/inch resolution. Figures 4.12 and 4.13 demonstrate addressability of the panel and show the excellent resolution and contrast of the on and off elements. The EL was excited at 120 volts rms (sine wave) and had a spot brightness of approximately 300 foot lamberts.

For comparison, a 500 x 500 per square inch sample was made using a powder phosphor. This sample was made with continuous electrodes on top and on the bottom. A layer of SiO_2 was evaporated on the bottom electrode. Holes were etched in the SiO_2 at the required resolution. Powdered phosphor was sprayed on with a plastic binder according to well known techniques. A continuous top electrode was then applied. An ac voltage applied between the front and back electrode shows the resolution capabilities of the powder. Figure 4.14 is the result. Although the phosphor and the electrodes are continuous, the phosphor does not emit light over the SiO_2 because of the additional capacitance provided by the SiO_2. Obviously the thin film EL is by far the better display medium.

5. CONCLUSIONS AND RECOMMENDATIONS

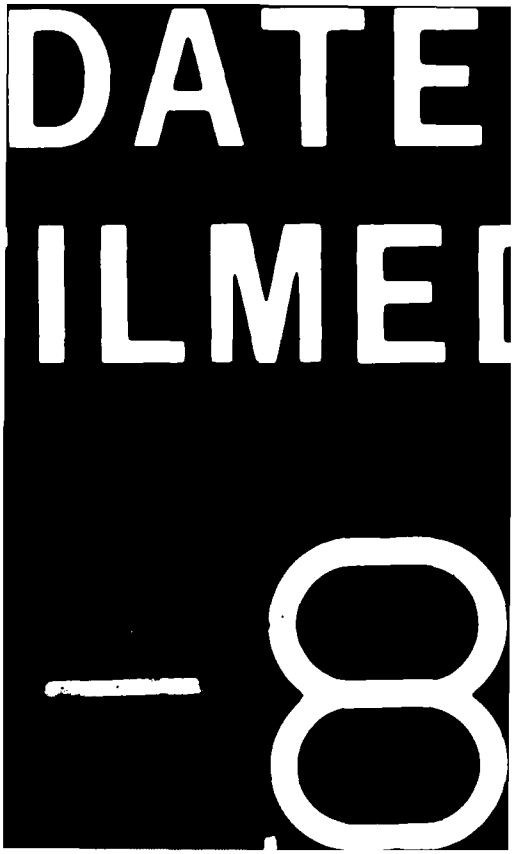
The principal conclusion to be drawn from the work presented here is that high resolution (500 lines/inch) matrix arrays, i.e. those incorporating thin film transistors for control of the matrix elements, cannot be produced with our present movable mask equipment (X-Y jig) because of the limited accuracy with which the mask can be set. With great effort, a 256 x 256 array could not be satisfactorily made with acceptable uniformity. Parts of the array function while other parts were too badly aligned.

We feel that the dedicated mask approach could be implemented successfully. However, the masks did not become available in time for the alignment procedures to be properly developed. The few alignment depositions that were made indicated some difficulty with mask expansion during insulator depositions. Further work in mask design and materials (e.g. masks with Kovar cores) plus the use of a pattern generator with finer resolution (Mann 3000 1 μm per step instead of Mann 1600 with 5 μm per step) could probably circumvent some of these difficulties.

Passive high resolution electroluminescent panels (500 x 500 panels per in^2) were made using both powder phosphors and thin film phosphors that demonstrate the superior resolution of the thin film display medium. The development of methods to incorporate a thin film phosphor with an active high resolution matrix are yet to be developed. The development of these techniques would contribute significantly to the quality and performance of the display.

6. ACKNOWLEDGEMENTS

The authors wish to acknowledge the contributions of A. M. Lewis and K. K. Yu, who were responsible for most of the work reported here. In addition, R. E. Stapleton, J. A. Asars, and M. W. Cresswell made important contributions, and Dr. T. P. Brody gave much initial guidance and support to the program, which the authors acknowledge. Further, the technical assistance of T. A. Brandis and G. J. Machiko in carrying out the depositions and of D. Leksell in fabricating passive electroluminescent devices is greatly appreciated.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